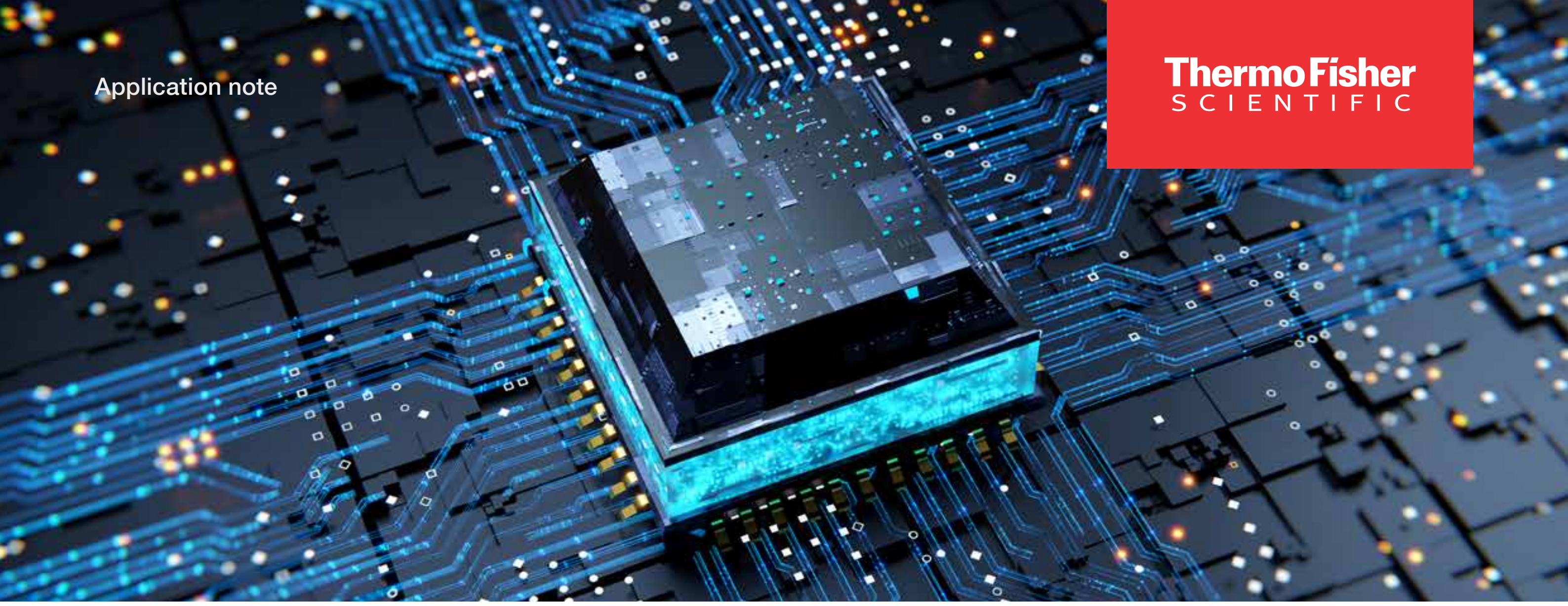

Optimizing high-current latch-up susceptibility and EOS testing

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Rethinking latch-up validation for high-current devices

As semiconductor devices continue to increase in complexity and operating current, validating their robustness under electrical stress has become increasingly challenging. Advanced processors, power devices, and multi-domain architectures introduce additional sensitivity to ESD and latch-up conditions. Consequently, test setup and execution can significantly influence results, where factors such as power sequencing, thermal behavior, and current delivery must be carefully controlled to avoid misleading outcomes. Accurate latch-up evaluation therefore requires both a detailed understanding of device behavior and a test approach that is capable of replicating realistic operating conditions with precision and repeatability.

Why accurate latch-up testing requires more than a standard setup

Latch-up is a complicated test used for complex electronics devices. Multiple power domains, device conditioning, power sequencing, and fixturing all must work together to get accurate results in latch-up. High current latch-up brings even further challenges such as thermal shock management, high-current fixture design, and the need for device temperature control.

While latch-up testing setup starts much the same way as ESD testing (i.e., by defining pin functions and grouping), it requires a deeper level of understanding of the device. Since the goal is to not have field returns, all possible scenarios must be considered. While typical latch-up failure will reveal an NPNP structure that acts as a short across a power plane and ground, it is also possible to have parasitic structures between power domains, or even IO pins.

Test fixture board design

Careful planning of latch-up tests starts with the design of the test fixture board.

a. If the DUT has more pins than there are channels available on the latch-up tester, consider grouping pins (ganging) into a single connection to reduce the number of channels required from the tester; grounds and power domains are usually chosen for grouping. Rotation should also be considered (if the device and socket allows it) to access different sets of pins for testing. Each position in the socket will require a different test plan, so care should be exercised when using this method. It is also possible to use multiple test fixture boards to test very high pin count devices. The tradeoff is cost and complexity, just as with rotation, as multiple fixturing requires multiple test plans. It is worth noting that ganging, rotation, and multiple fixtures can be combined.

b. High-current fixtures must be able to safely handle the current applied to the device. This might require heavier copper layers, and, in some cases, multiple planes tied together for power and ground. Additionally, ground requires special attention if multiple high-current supplies are used that share a common ground. In this case, the ground copper layers must be able to handle the sum of the combined power currents. The maximum allowed temperature rise also needs to be considered. An overview on these calculations can be found in Peterson (2021).[1]

c. High-current cables are typically attached to the test fixture board using bolts, which, together with the power and ground planes, need to be able to carry the test current safely. The ability of a bolt to carry current depends on its material and size. It is often best to solder the bolts to the PCB. The nuts and bolts must also be properly torqued.

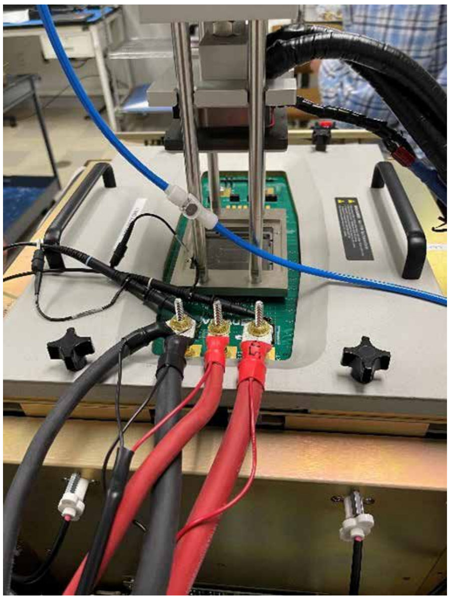


Figure 1. High-current cables attached to the test fixture board using bolts.

d. Large cables will exert a downward force due to their weight and tension on the PCB; a tension reducing technique should be implemented to extend the life of the test PCB.

e. The device socket material must be able to withstand the test temperature; the socket, in most cases, should manage the temperature of the device (see ***Device activation and thermal control*** section, below).

Power sequencing

Every device that uses multiple power supplies requires careful sequencing, as power supplies must be turned on in a way that prevents potential biasing of parasitic structures. In general, the device designer should be able to provide proper power sequencing in order to avoid latch-up conditions. There are three common power-up sequencing techniques:

1. **Simultaneous power up:** all power supplies are turned on at the same time and at the same slew rate.

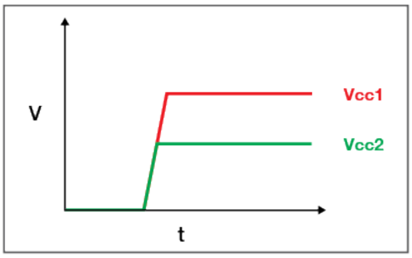


Figure 2. Simultaneous power up of two power supplies.

2. **Sequential power up:** one power supply is turned on at a time. Sufficient time is allowed for each power supply to reach its operation point before another power supply is turned on.

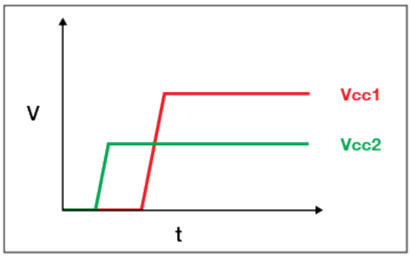
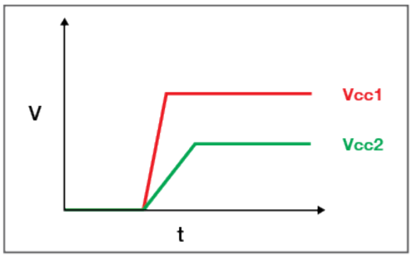


Figure 3. Sequential power up using two power supplies.

3. **Ratiometric power up:** one or more power supplies are turned on at the same time, but with different slew rates that allow for a fixed V1/V2 ratio.



4. Ratiometric power up using two power supplies.

Device conditioning (vectoring)

Complex devices may have more than one mode of operation (i.e., normal, boosted, power-saving, etc.), which can be controlled through register values. Such changes in programming could cause normal fluctuations in operational current that should not be confused with latch-up events. To prevent any false positives for latch-up, it is imperative that the device is in a known state during the analysis. This is accomplished by first loading vectors to registers or memory in order to condition the device. The vector system must have a known depth (number of bits sent to an I/O pin) and frequency to be effective.

Device activation and thermal control

Care should be taken when a high-current device is turned on, as the heat produced by the current flow could cause a fast rise in temperature. If this is not controlled, temperature gradients inside the device could cause physical damage due to thermal stress. There are two general ways to control turn-on thermal shock:

1. Power supply turn-on slew rate control. A power supply used to test latch-up susceptibility must have a fast slew rate that allows for stress pulses down to single millisecond widths. Although this may be desirable during the stress testing itself, it could be a problem during initial device turn-on, where a rise time of less than 1 millisecond could cause excessive thermal stress and possible physical damage (such as fractures). To prevent this, it is necessary to have a power supply that can control its turn-on slew rate to reduce thermal stress.

Figure 5. Power-up slew rate, programmed to 1 msec using MK.4TE Scimitar Software and the high-current power supply option.

2. Device pre-heating. Heating the device before it is turned on can potentially reduce thermal stress. This requires a socket with an integrated electric heater, or the use of a thermal stream.

Since latch-up susceptibility is dependent on temperature, it is imperative that the device is kept at a constant temperature during testing. For high-current latch-up tests, a thermal management system is necessary. This can be done with forced air in a thermal stream, or through a socket with a water-cooled jacket and an electric heater. Note that this socket would need to be specially designed for a given device. The combination of water-cooled jacket and electric heater typically produces more stable temperature control than forced air.

Four quadrant power supplies

Latch-up is generally thought to occur between a power rail and ground, as shown in **Figure 7**. In a device using multiple power domains, it is also possible to have a parasitic structure turn on between two power domains. For this susceptibility to be detected, the power supplies, as shown in **Figure 8**. used for the latch-up susceptibility testing must be able to source and sink current on both polarities. These are known as four-quadrant power supplies; using power supplies with only one or two working quadrants might mask a latch-up susceptibility and produce a false negative.

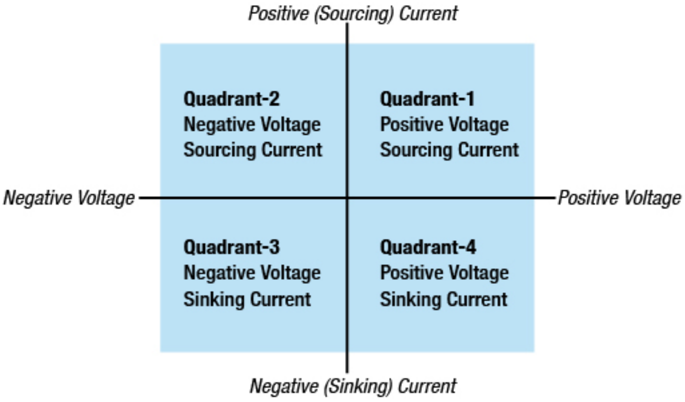


Figure 6. A four-quadrant power supply that can source and sink current in both polarities.

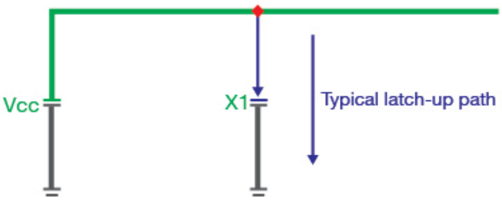


Figure 7. Typical latch-up current path through a parasitic SCR structure.

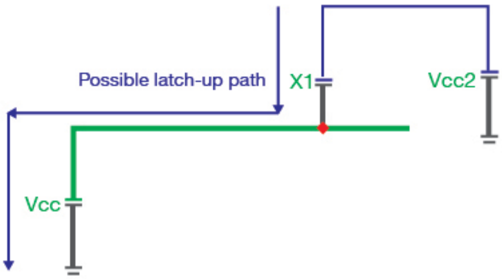


Figure 8. Possible latch-up path between two power domains.

Power supply current budget

It is necessary to plan the total current needed for proper testing, keeping in mind that the device needs to be stressed to 1.5x its normal operating voltage (per JESD78; maximum allowed limits should not be exceeded).[2] It is possible that the device will need 1.5x the current as well. Note that all power supplies have limits; it is best to keep power supplies operating below 95% of their current and voltage capacity, as this helps ensure that the power supply can control its output.

Example: A test device that has a normal operating current of 100 A will require a power supply of at least (100 A x 1.5)/0.95 = 157.89 A.

Key requirements for high-current latch-up testing

High-current latch-up susceptibility testing has all the requirements of standard latch-up testing, with added considerations for high current, including:

1. TFB design
2. Thermal management
3. Proper vectoring (device conditioning), when necessary
4. Power supply selection
5. Current budgeting

Thermo Scientific MK.4TE and MK.2TE ESD and Latch-up Test Systems, when combined with the high-current power supply option, fully support high-current latch-up testing, offering:

1. External vectoring using JTAG or parallel data lines (up to 128)
2. Up to 7 high-current power supplies (each from 125 to 750 A)
3. Programmable turn-on and stress-rise time
4. Stress in the range of low-single-millisecond pulses
5. Integrated programming and results

Improving confidence in latch-up test results

High-current latch-up testing presents a combination of electrical, thermal, and system-level challenges that must be addressed to help ensure reliable results. As device current requirements increase, traditional test approaches may no longer provide sufficient control or accuracy. Proper test fixture design, power sequencing, thermal management, and current capability all play critical roles in capturing true device behavior. A well-integrated test solution, like the MK.2TE or MK.4TE Test System, enables consistent execution and reduces the risk of false positives/negatives. By aligning test conditions more closely with real-world operation, engineers can increase their confidence in qualification results and reduce the likelihood of downstream reliability issues.

References

1. Peterson, Z. How to Calculate PCB Power Plane Current Capacity. Altium (2021). URL: https://resources.altium.com/p/how-calculate-pcb-power-plane-current-capacity
2. IC Latch-up Test. JEDEC (2023). Doc #: JESD78

Learn more at **thermofisher.com/latch-up-test-system**