APPLICATION NOTE

Transforming failure analysis of wide bandgap power MOSFET devices

Improved defect localization and failure analysis tools

As the dimensions of semiconductor devices shrink and become more complex, defect localization and failure analysis become more critical—and more challenging. With structural elements such as high-density interconnects, wafer-level stacking, flexible electronics, and integral substrates, failure-inducing defects have more places to hide. Even worse, these failures can occur at the device packaging stage, resulting in decreased yield and increased time-to-market.

These challenges have become especially important in the area of power electronics. Electric vehicles (EVs) are a noteworthy example, requiring power components that provide greater performance, exceptional efficiency, and reliable high-temperature operation in a small package. Reliability is especially important in vehicles that may be travelling at highway speeds.

For designers, a combination of electrical failure analysis (EFA) and physical failure analysis (PFA) can lead to a deeper understanding of fault mechanisms and, ultimately, improved manufacturing yield along with enhanced operational performance and reliability. Thermo Fisher Scientific offers advanced analytical tools for fast EFA and PFA. When combined into a complete EFA-to-PFA workflow, these tools allow you to localize and characterize subtle electrical issues in wide bandgap materials such as gallium nitride (GaN) and silicon carbide (SiC).

Utilizing new materials in power devices

Wide bandgap power devices are well-suited to demanding applications, such as EVs that require high power, or Internet of things (IoT) designs that need exceptionally long battery life. Unfortunately, materials such as GaN and SiC can experience failure modes that developers have not seen previously. As a result, traditional approaches to fault analysis may not be up to the task. This makes it more difficult to identify the root causes that can affect yield and reliability.

Silicon metal-oxide semiconductor field-effect transistors (MOSFETs) provide a useful example. Designed for high-power applications, these have been the go-to devices for a majority of switching-power applications. Unfortunately, the performance of power MOSFETs has reached a limit, as new requirements demand higher voltages and faster frequencies in smaller form-factor packaging. Redesigning such devices using GaN or SiC has enabled the creation of reliable, compact, and cost-effective solutions for emerging high-power applications.

Stating the problem: Failures in power MOSFET devices

When fabricated using wide-bandgap materials, power MOSFETs have a vertical structure that places sources and drains on opposite sides of the wafer, enabling higher current and voltage bias. Note that this is different from CMOS devices, which use a parallel structure.

In the electrical realm, leakage currents between drain and source (IDSS) or between gate and source (IGSS) are general categories of failure in power MOSFETs. The ability to focus failure analysis on these mechanisms provides important insights that can be used to improve production methods, production yields, and future designs.

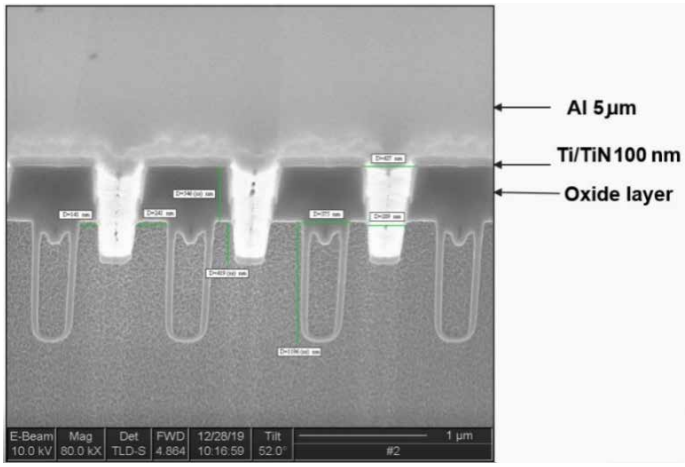

Figure 1.Electron-beam image showing drain side of a power MOSFET wafer with aluminum deposited on top of the titanium/titanium nitride layer.

In the physical implementation, metal layers of aluminum (Al) and titanium (Ti) or titanium nitride (TiN) are typically deposited on top of individual transistors (Figure 1). These opaque layers can create difficulties in fault isolation. For example, it is difficult to use a photon-emission microscope (PEM) or optical beam induced resistance change (OBIRCH) scanning to accurately observe or locate defects. Photons cannot penetrate the layers of metal, and the metals might absorb the OBIRCH laser light.

Outlining an EFA-to-PFA workflow

This set of challenges makes a strong case for an analysis strategy that includes both EFA and PFA. When used in combination, the strengths of EFA and PFA enable rapid localization, isolation, and visualization of electrical and physical faults.

From our work with power-device manufacturers, we have developed a four-part workflow that progresses from EFA to PFA: coarse fault isolation, sample preparation, fine fault isolation, and imaging and analysis.

- Coarse fault isolation: In a power MOSFET, failure may be due to IDSS or IGSS leakage currents. This step uses lock-in thermography (LIT) to localize defects (Figure 2).

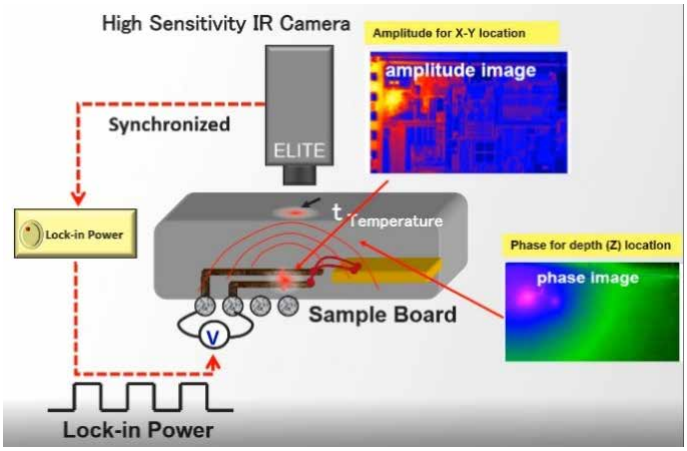

Figure 2. Coarse fault isolation, which identifies heat distribution on the surface of a wafer, can be performed using lock-in thermography.

- Sample preparation: This begins with de-processing, which uses the plasma focused ion beam (PFIB) method to remove the top layers of aluminum and Ti/TiN
- Fine fault isolation: This step uses one- or two-tip nanoprobing to isolate the failure location (Figure 3).
- Imaging and analysis: To enable PFA, these rely on current/voltage (IV) characterization to confirm the electrical failure of a specific device. A sample is prepared using focused ion beam (FIB), then a scanning electron microscope (SEM) or transmission electron microscope (TEM) is used to observe and analyze the physical defect.

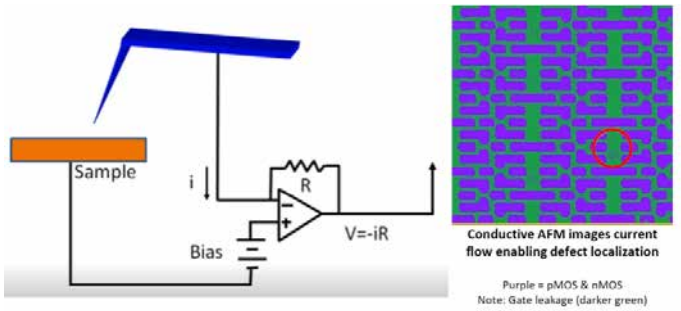

Figure 3. Fine fault isolation can use current probing (left) to produce a two-dimensional current map (right) of the wafer under test. Color is used to show current level, and in this example, the darker green area within the red circle highlights gate leakage.

Applying the workflows: Two case studies

A pair of case studies illustrates the advantages of this approach. **Case #1** explores an actual IDSS leakage failure, and **Case #2** examines an I_{GSS} leakage failure.

Examining case study #1: I_{DSS} leakage failure mode

The results of a chip-probing (CP) test indicated low yield in the wafer under test. Three die were chosen for further failure analysis (Figure 4).

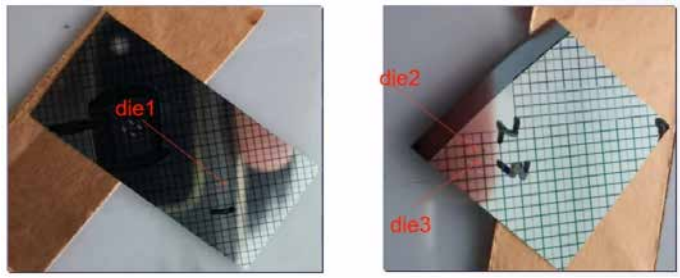

Figure 4. Two pieces were cut from the wafer under test to enable further testing and analysis.

During testing, the source and gate voltages were set to zero. Next, a force sweep of drain voltage, Vds, was performed from zero to twenty volts, and Ids was measured at 10 V. Graphs for each die reveal high leakage current at low voltages (Figure 5).

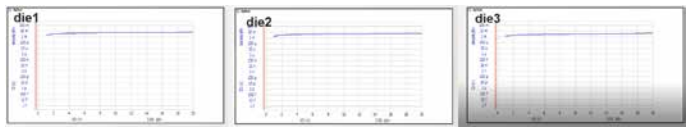

Figure 5. Force-sweep measurements on all three die revealed high leakage current between source and drain.

Two die were then chosen for total failure analysis. The first step was to perform photo isolation using the Thermo Scientific™ ELITE System and the Thermo Scientific Hyperion II System*. IV characterization (Figure 6) confirmed the high level of leakage from drain to source (IDSS). The analysis then proceeded using the four-step workflow.

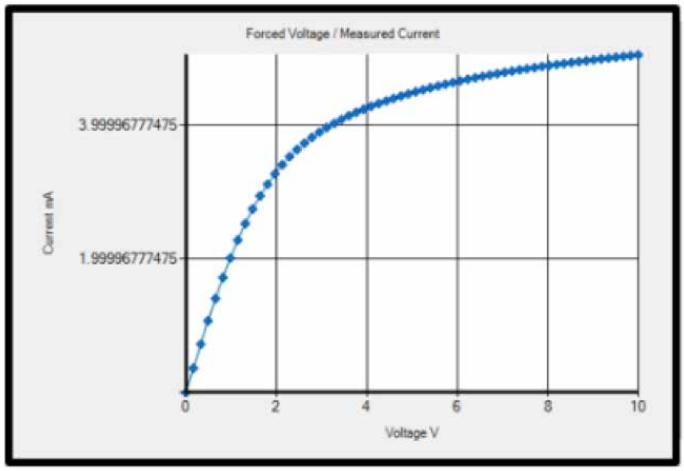

Figure 6. A measurement of sample die #1 confirmed the high level of I_{DSS} leakage.

Coarse fault isolation: The ELITE System detected hotspots through the thick top layer of metal. However, a 4 µm spot encompasses many underlying devices. Thus, it was necessary to further isolate the defect to narrow down the target. ELITE software was used to measure from the edges to the hotspot (Figure 7), and this information enhanced navigation in the next step when using the Thermo Scientific Helios™ 5 PFIB DualBeam during de-processing.

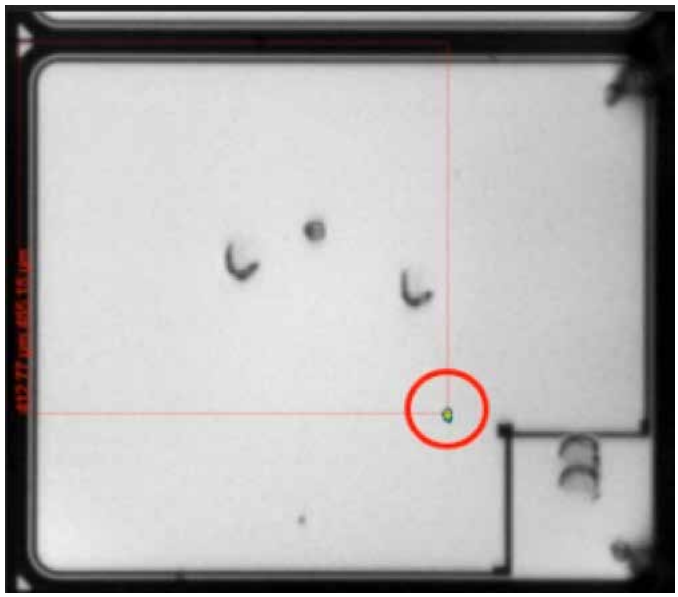

Figure 7. Thermal imaging provided coarse isolation of the hotspot. The location was measured from edges of the device.

Sample preparation and de-processing: Next, the Helios 5 PFIB DualBeam was used to remove a 100x100 µm window of the thick Al layer and the thinner layer of Ti/TiN. This exposed the source counter, as shown in Figure 8.

* The appendix at the end of this document includes information about relevant Thermo Fisher solutions.

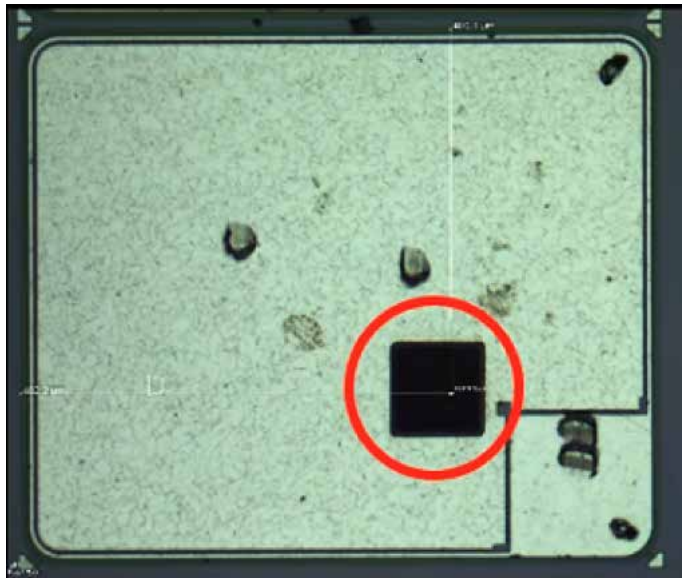

Figure 8. After PFIB, this optical microscopy (OM) view from the Hyperion II System shows the source counter within the device.

Fine fault isolation: The Hyperion II System was used to scan a 5x5 µm square around the hotspot, and a PicoCurrent image covered the failed source contact (Figure 9, left). The failure was localized with the chuck biased at 0.25 V and with zero bias at the tip and gate. This was compared to the topographic image (Figure 9, right, from the Hyperion II System), and probing was then used to confirm the fault using the Hyperion II System. The test conditions were sweep from –1 to +1 V; drain and gate bias fixed at zero volts; and current compliance at 10 µA.

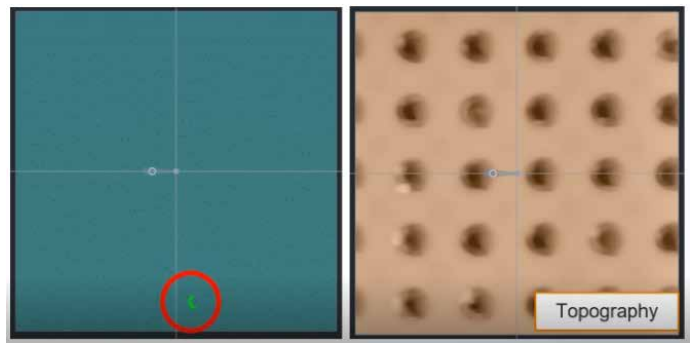

Figure 9. The PicoCurrent image (left) was produced using a 5x5 µm scan size. The red circle highlights the region of high leakage current.

Imaging and analysis: Fault navigation and PFA matched the failure address, as shown at the left in Figure 10. The number of failed contacts was counted, and the system produced an image of the actual defect (right side of Figure 10). The contrast in the final image was enhanced using Insulator Enhanced Etch (IEE) with xenon difluoride gas.

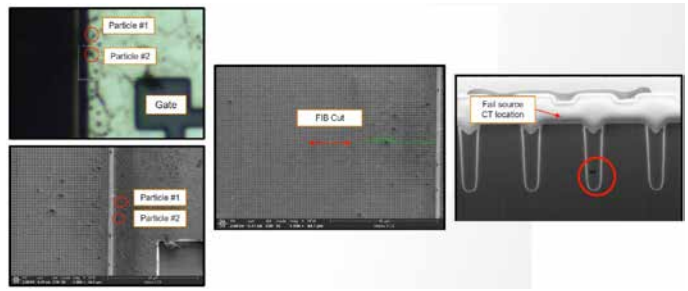

Figure 10. The process proceeded from fault navigation (left) to a FIB cut (center) and then an image of the actual defect, which is a failed source contact (right).

Examining case study #2: I_{GSS} leakage failure mode
This analysis was performed on a different wafer under test that was also suffering from low yield, as shown using a CP test. The wafer map shows the occurrence of I_{GSS} failure (Figure 11).

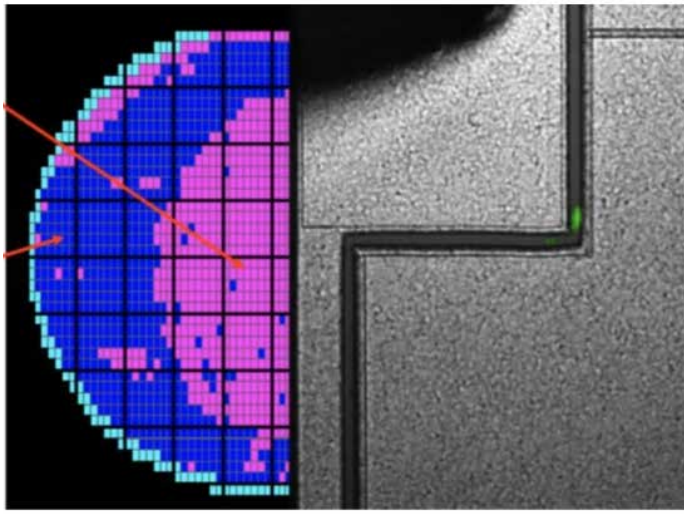

Figure 11. The wafer under test was experiencing high levels of I_{GSS} leakage.

The initial investigation used OBIRCH to perform photo isolation, but this did not provide an accurate location for the application of PFA. Next, IV characterization was performed on four edge die, and all had suffered IGSS leakage failures. Specifically, leakage was very high when the gate was at 1 V.

Coarse fault isolation: Next, lock-in thermography was used to localize the defect. As shown in Figure 12, this revealed two hotspots at the gate corners (using the ELITE System).

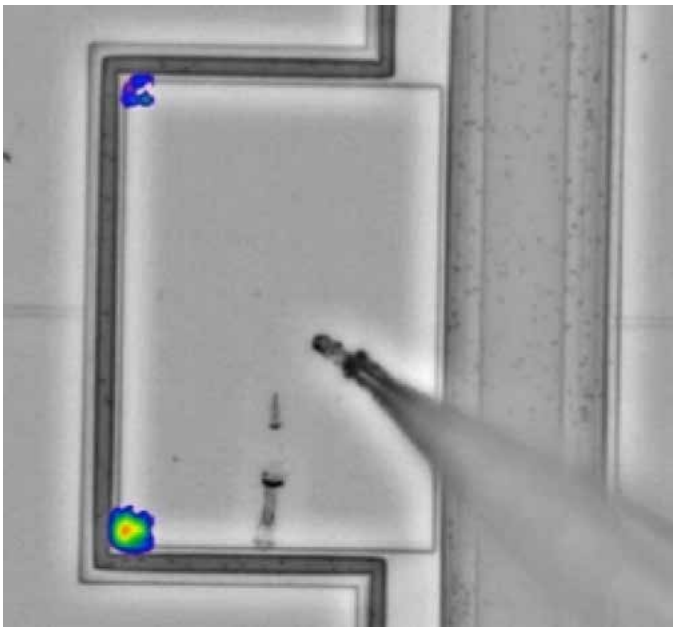

Figure 12. Because OBIRCH was not accurate, a second experiment was performed to more accurately locate the thermal hotspots.

Sample prep: The Helios 5 PFIB DualBeam was used to perform de-processing in two ways: without and with Dx gas (Figure 13). DX gas is our unique approach to the deposition or delayering of sample materials. For example, it enables precise removal of layers, access to areas of interest, and exposure of defects.

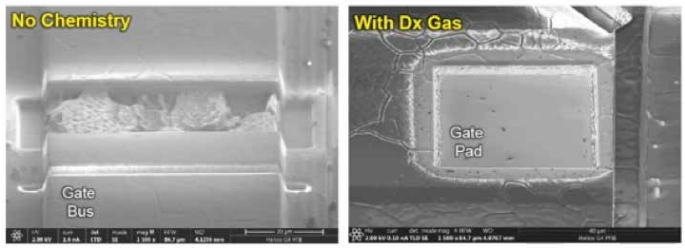

Figure 13. The addition of Dx gas flow provided significant improvement in the planarity of PFIB de-processing.

In this case, the addition of Dx gas flow provided significant improvement in planarity of the PFIB de-processing. This effectively eliminated the need for crystal orientation-mediated differential milling, which typically produces non-uniform delayering. The combination of Dx chemistry and PFIB provides a unique, site-specific approach that makes it possible to open up relatively large windows into the aluminum layer to more easily hunt for the defect-causing fault.

Fine fault isolation: The application of PFIB de-processing clearly exposed the tungsten metal lines, as shown in the two pullout images in Figure 14. Once again, the ELITE System was used to capture the hotspots, and these occurred at the corners of the tungsten lines (small blue circles in the main part of Figure 14).

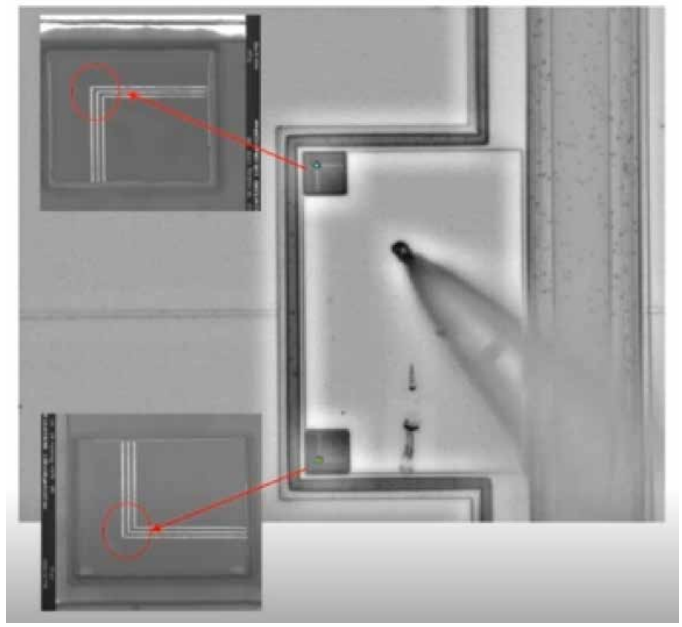

Figure 14. The Helios 5 PFIB DualBeam's de-processing produced excellent uniformity in the exposed areas.

Final analysis: Figure 15 shows the final results of the PFA process. These side-view images compare the failure site (upper) with a reference site (lower). In the failure site, there is a short between the tungsten lines and the substrate, as seen at the right in the upper image.

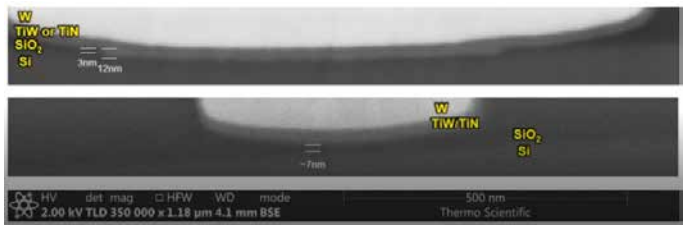

Figure 15. At the upper-right, the edge-most line is shorted to the substrate.

Results

These cases illustrate the extent of the total solution we can provide for a combined EFA-to-PFA workflow. In both examples, the EFA process isolated the fault, and PFA data successfully visualized and verified the defects at the respective fault locations.

With each sample, the ELITE System detected a single heat source through the thick aluminum layer. PFIB de-processing removed squares of the aluminum and Ti/TiN barriers quickly and uniformly, providing an excellent surface for nanoprobing. PicoCurrent imaging using the Hyperion II System was used to scan multiple source contacts, and this enabled isolation of faults at nano scale. Simultaneous electrical testing with the biased chuck verified the fault locations.

PFA achieved a 100-percent success rate using specific surface particles and contact counting to navigate to the fault sources. The gas injection system (GIS) with IEE helped enhance the contrast between silicon and oxide.

This innovative approach is another example of our commitment to enabling you to push science and technology a step beyond. For more information, please visit the Semiconductor Analysis section of our website.

Appendix: Profiles of key products

ELITE System: Rapid growth in advanced packaging applications, complex interconnect schemes, and higher performance power devices, is creating unprecedented challenges in failure localization and analysis. Defective or underperforming semiconductor devices often show an anomalous distribution of local power dissipation, leading to localized temperature increases. The ELITE System utilizes Lock-in IR Thermography (LIT) to accurately and efficiently locate these areas of interest.

Compared to steady-state thermography, LIT is a form of dynamic IR thermography that provides a much better signal-to-noise ratio, increased sensitivity, and higher feature resolution. LIT can be used in IC analysis to locate line shorts, ESD defects, oxide damage, defective transistors and diodes, and device latch-ups. LIT is performed in a natural ambient environment without requiring light-shielding boxes.

Helios 5 PFIB DualBeam: The Helios 5 Plasma FIB (PFIB) DualBeam focused ion beam scanning electron microscope (FIB-SEM) delivers unmatched capabilities in semiconductor and materials science applications. For manufacturers of semiconductor devices, advanced packaging technology, and display devices, the Helios 5 PFIB DualBeam delivers damage-free, large-area de-processing, fast sample preparation, and high-fidelity failure analysis. For materials science researchers, the Helios 5 PFIB DualBeam provides large-volume 3D characterization, gallium-free sample preparation, and precise micromachining.

Helios 5 DualBeam: The Helios 5 DualBeam builds on the high-performance imaging and analysis capabilities of the industry-leading Helios DualBeam family. It is carefully designed to meet the needs of materials science researchers and engineers for a wide range of focused ion beam scanning electron microscopy (FIB-SEM) use cases—even on the most challenging samples.

Hyperion II System: The Hyperion II System offers fast, accurate transistor probing for electrical characterization and fault localization in support of semiconductor technology development, yield engineering, and device reliability improvement. The unparalleled stability of the Hyperion II System enables nanoprobing down to the 5 nm technology node and beyond.

The Hyperion II System's stable production medium (SPM) technology enables PicoCurrent imaging, which is a way to rapidly identify shorts, opens, leakage paths, and resistive contacts with more than 1,000 times the sensitivity of passive-voltage contrast techniques. The scanning capacitance microscopy (SCM) module provides image-based fault localization for silicon-on-insulator (SOI) wafers, as well as high-resolution dopant profiling.

nProber IV System: The Thermo Scientific nProber IV System is a high-performance SEM-based platform for the localization of transistor and metallization faults. The system directly increases the success rate of TEM analysis through precise fault localization and has proven to be both accurate and repeatable on even the most challenging process nodes. The automation and guided workflows of the nProber IV System improve lab productivity and allow your organization to focus on the output of your nanoprobing and TEM workflows while investing less in the operation of the system itself, thereby accelerating time-to-yield.

NEXS Software: Thermo Scientific NEXS Software enables diverse workflows by providing CAD connectivity with Thermo Scientific analytical equipment. It directly reads and displays mask data and accurately drives the system stage to fault or edit locations. In addition, NEXS Software goes far beyond the capabilities of CAD viewers and stage drivers by facilitating fault isolation, failure analysis, sample preparation, and circuit edit.

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Notes

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