WHITE PAPER

The challenge of measuring buried critical dimensions in high-aspect-ratio structures

How busy fab process owners can reduce time-to-data in 3D NAND metrology

Abstract

Innovation in advanced memory architectures is driven by the data demands of applications like IoT, artificial intelligence, ADAS, and big data analysis. To meet this demand, memory manufacturers are striving to increase the bit-density of their products, which means tighter pitch and taller structures. With these requirements, the critical features become high-aspect-ratio (HAR) channel, or memory, holes that are becoming taller and narrower, pushing the limits of process control to minimize problems like bow, twist, and tilt along the hole length.

Metrology, the process of measuring these critical dimensions (CD), stands out as one of the main technological challenges. It is difficult to measure CDs of HAR structures in 3D NAND, as the structure of the memory layers does not allow conventional metrology equipment to access these features throughout their depth, especially in the middle regions and the bottom of the stacks. Legacy metrology tools have limitations, leaving manufacturers without a method to accurately measure HAR structures quickly. Ultimately, this adds up to more cost, process complexity, and delays in bringing the next technology to market.

This white paper outlines two main challenges associated with 3D NAND development, both of which lead to reduced yield and process delays: (1) the difficulty of accessing buried sites in HAR structures, and (2) the slow turnaround from using metrology labs. It also outlines how fabs are dealing with these problems and why current technology is insufficient going forward. This white paper then discusses how the above issues can be solved by adopting lab techniques and technologies into automated inline metrology solutions directly in the fab.

Introduction: Pushing the boundaries of memory and storage

Driving innovation in advanced memory

According to VLSI Research, the overall NAND market is expected to reach $57 billion (USD) in terms of sales in 2021, an increase of 12% over 2020[1, 2]. And according to Global Market Insights, the semiconductor memory market size topped $100 billion in 2019, with forecasts predicting it will rise further at a CAGR of more than 13.8% from 2020 to 2026[3].

Driving this growth are increasing amounts of data and applications requiring fast access to this data, such as AI, edge computing, high frequency trading, and ADAS/ autonomous vehicles. For example, according to the IDC's Global DataSphere Forecast, more than 59 zettabytes (ZB) of data were created, captured, copied, and consumed worldwide in 2020[4]. Not only this, but the amount of data created over the next three years will be more than the data created over the past 30 years.

Ultimately, the explosion of data means there is a constant drive to push storage capability beyond what is currently available. In other words, performance and capacity must be improved if memory technology is to keep up with demand[5].

What does this mean for 3D NAND?

For 3D NAND manufacturers, this translates into the need to add more layers with each generation and pack more bits into tighter spaces to meet performance, latency, and capacity demands. According to Mark Webb at MKW

Ventures Consulting, 30% to 50% more layers are being added for each 3D NAND generation[6]. With each successive generation adding multiple additional individual processes to take a raw wafer to a completed die, the potential for problems also increases.

For example, Micron recently announced their 176-layer NAND, which is close to ten times denser than the earliest designs[7]. And while ten times the density enables mobile devices and other applications to do more and store more data, it also results in added design, manufacturing, and metrology complexities.

So the challenge becomes measuring CDs that are buried deep within the stacked layers.

The challenge of accessing buried structures in 3D NAND

With planar NAND, metrology was relatively straightforward, as it employed top-down analysis techniques to measure features that were directly visible. However, with 3D NAND, the profiles, channels, layers, and defects are buried within the device—not on top. The resulting challenge is that most metrology tools are unable to go through the structure and look inside to perform the necessary measurements[8].

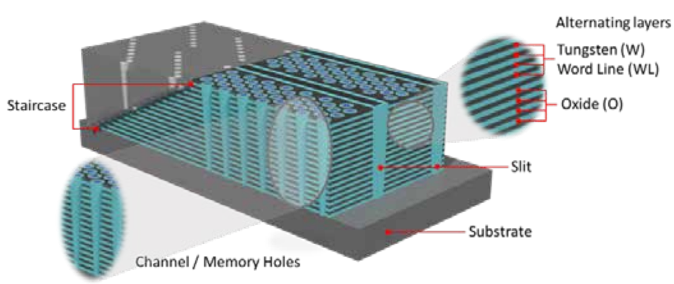

Figure 1. Anatomy of 3D NAND.

For example, the channel hole etch is the foundation step around which 3D NAND is designed. Controlling the geometry of the channel hole is crucial to both the yield and reliability of the device. The etch process to create these channels is also one of the main challenges for current and future 3D NAND designs, according to TechInsights[10].

Measuring CDs along the channel length is crucial, because variations in the channel holes can have drastic effects on the performance of 3D NAND devices. A study in Microelectronics Journal showed an increase in channel resistance due to narrowing of the poly-silicon channel width[11]. In turn, the authors recorded a reduction of on-current by 19% for an etch angle of 89.2. Additionally, the degradation in cell characteristics became worse with an increase in the number of word lines. The authors concluded that CDs need to be controlled to reduce etch angles due to the on-current degradation.

To stay competitive, manufacturers are using other techniques to extend the depth of their etch. One of the adopted techniques is multi-deck stacking. This technique revolves around repeated oxide-nitride-blocking oxide (ONO) deposition and channel hole reactive ion etch (RIE) to build up the structure in "decks." By doing this, manufacturers can ensure better maximum channel hole etch performance while extending their layer count via decks. The cost for this process, however, is the additional number of process steps, as the wafer makes multiple passes through the etch.

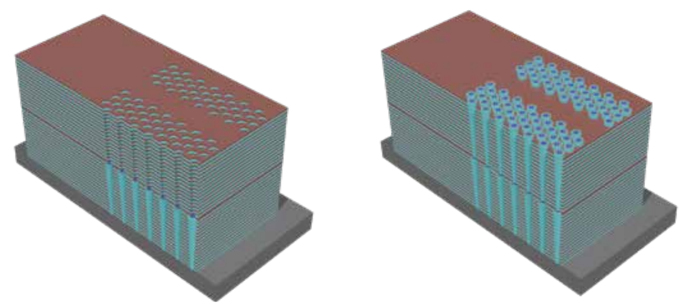

Figure 2. 3D NAND fabrication process.

Adding to this complexity is the deck-to-deck channel hole overlay for multi-deck products. This refers to the placement of two channel holes in relation to each other when aligning one stack on top of another. The process involves aligning a hole, typically 80–100 nm in width and drilled through several microns, on top of another hole that is the same width. This is an incredibly challenging process to get right trillions of times.

Metrology challenges

As a 3D NAND's vertical structure increases in height, metrology becomes increasingly critical. Each successive node transition lengthens the manufacturing process, with the role of metrology expanding to include exploratory research, technology development, yield learning, and process monitoring. For metrology analysis, the ability to see into the 3D device to measure and characterize the structure and pinpoint problems is critical to increase yield, reduce manufacturing costs, and accelerate time to market.

Of the processes, the channel hole HAR etch is arguably the most difficult step and adds considerable challenges.[9] The channel hole profiles need to be measured, including the top and bottom CDs of the holes, as well as inside the channel. Any variations in channel hole width from top to bottom need to be characterized[12], and problems such as bow CD, twist,

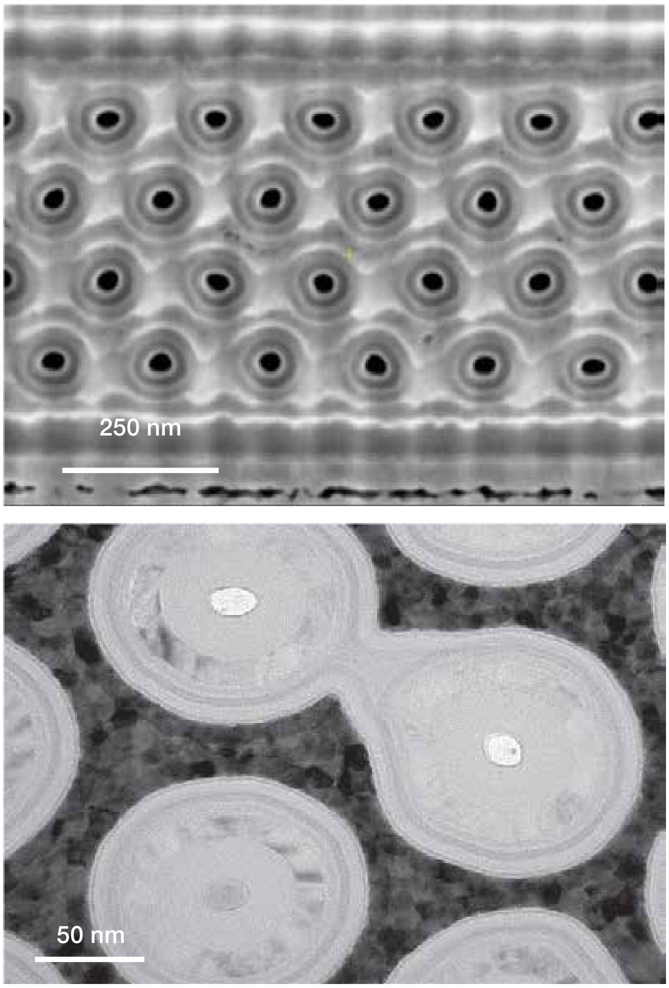

Figure 3. Filled (top) and partially filled (bottom) structures on a 3D NAND device.

and tilt need to be identified. To further complicate this process, as the etch depth increases, etch rates tend to decrease, which can exacerbate these problems.[10]

Ideally, for channel holes, 3D NAND manufacturers need metrology tools with the ability to accurately measure CDs inside the channel at each layer. This is critical for process control and to improve performance and yield. However, accessing buried critical dimensions is not the only problem with current metrology tools.

Transferal of samples to a metrology lab involves significant cost

Before metrology is performed on memory devices, wafers are typically transferred to a lab. The goal is to characterize and measure CDs within a new 3D NAND design, helping vendors gain a thorough understanding of any problems or defects in the process workflow. The problem is that the lab and fab usually work in silos.[13] And while the lab can provide advanced analytical solutions, the transferal of samples from fab to lab is slow.

In addition to the transit time, the analysis itself can be time-consuming. As labs are shared between different groups, time to data can be impacted by lab case queueing and management. The process or integration engineer is at the mercy of the prioritization system inherent in a lab environment. Since time to data is slow when using a metrology lab, the fab engineer must continue doing experiments themselves to try to “pre-solve” the problem and fall back on data they finally receive to validate their decisions.

Clearly, to further improve time to market, 3D NAND fabs need to adopt some techniques and technologies that have historically only existed in lab environments.

Current fab metrology tools are not the “whole” solution

As mentioned, advanced memory manufacturers continue to use the same metrology tools for both planar and 3D NAND. Unfortunately, these solutions are sub-optimal, as they are unable to completely access 3D NAND’s vertical structure and perform necessary measurements. Instruments used for this kind of metrology include CD-SEMs, optical CD (OCD) equipment, overlay systems, TEMs, model-based infrared reflectometry (MBIR), and X-ray tools[15], with OCD being the most common[9]. While each of these tools has its benefits and tradeoffs, no single instrument provides a complete metrology solution for 3D NAND. The following provides a summary of each metrology technique and its advantages and weaknesses.

OCD

OCD leverages scatterometry and uses a model-based analytical technique in which the actual features or critical dimensions are not measured directly. Instead, a model is developed based on very specific parameters to interpret the scatterometry data. Experimental results are then compared with the model to determine critical dimensions as accurately as possible[9].

Scatterometry is able to extract discrete CDs when measuring optically transparent blanket film stacks. However, when measuring tall, complex HAR structures in three dimensions, the resulting data is too convoluted to extract precise measurements. Data gets “mapped” to results from known feature configurations through modeling to provide an “indicator” of structural characteristics. This makes OCD useful for quick validation measurements, but not as a direct measurement tool.

OCD does have a specific advantage over other methods: speed. But it should be noted that the models needed to interpret the results are complex and take significant time to develop. The technique is also limited to the top layers of the device, as its light source cannot penetrate the full stack, meaning that it cannot analyze structures below the top few layers. Finally, the technique also comes with significant measurement uncertainty because of the model complexity, as well as the need to constantly check reference data to ensure accuracy.[15, 16]

CD-SEM

Unlike OCD, CD-SEM involves direct metrology, making it fast and straightforward to use. It is also a low-cost technique and already installed in many fabs for other analysis needs. CD-SEM can be a viable method for measuring the tunnel ONO film thickness in 3D-NAND devices.[17] The ONO film thickness affects device properties, and so it is crucial to measure this feature accurately.

However, while CD-SEM may be useful for measuring ONO film thickness, it is unable to measure complete channel hole profiles or features buried deep within the stack. The main CD-SEM shortcoming is, like OCD, that it can see only the top layers of a device or, in a very limited fashion, measure the top or very bottom of an unfilled channel hole. This results in the inability to provide essential information through the entire stack.

CD-SAXS

Critical dimension small angle X-ray scattering (CD-SAXS) is a variable angle, transmission X-ray technique. X-rays are scattered from periodic nanostructures and can be analyzed to determine the dimension and shape of HAR features.[9, 18, 19] The method is non-destructive and is sensitive to 3D HAR structures because the X-ray scattering strength depends on the square of the height of a structure. This means high-aspect-ratio structures scatter more strongly than features with a low aspect ratio. As a result, various studies have shown that CD-SAXS is useful for advanced memory metrology[19].

However, there are three main downsides. The first is the expense, with CD-SAXS tools costing much more than comparative tools like OCD and SEM.

The second downside is that direct metrology is not performed when using CD-SAXS. In practice, the technique does not image the individual features and extract specific critical dimensions. Rather, 3D NAND CDs are inferred based on the series of transmission spectra when compared to the model. As a result, the measurement is an average of the sample location's CDs. While useful from a statistical, global perspective, it does not provide the whole picture. This can lead to measurement uncertainty similar to other model-based approaches like OCD. And depending on the complexity, these models can be time-consuming to create and validate.

Finally, the tool is relatively slow compared to CD-SEM and OCD. Its X-ray source is limited in both photon energy and count, which means that more time must be spent at each site to extract sufficient data to create an analysis. This is a major challenge to the technique. And while higher flux and power sources exist, they drastically increase both the cost and size of the CD-SAXS apparatus.

Introducing the Helios 5 PXL Wafer DualBeam

To address the metrology challenges of 3D NAND, a better workflow solution is needed. 3D NAND manufacturers require precise and accurate data faster, to drive process improvements, maximize yield, and reduce time to market. Specifically, fab process owners need deep insights into the internal profiles and CDs of 3D NAND structures with lab metrology technologies in the fab.

The Thermo Scientific™ Helios™ 5 PXL PFIB Wafer DualBeam is a combination xenon plasma FIB-SEM tool that performs FIB metrology techniques rapidly on full wafers. This enables fab metrology engineers to gather data, on a fully automated tool, that has historically been accessible only via the lab.

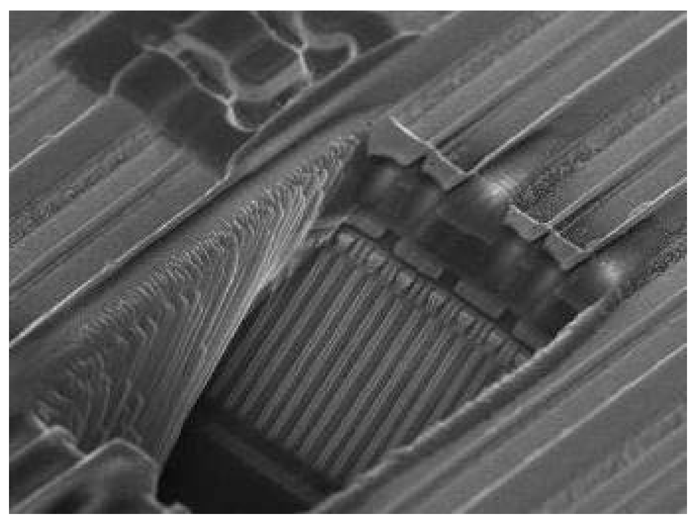

Figure 4. Wide-area diagonal mill of 3D NAND device.

A primary capability of the Helios 5 PXL PFIB Wafer DualBeam is diagonal milling. Diagonal milling rapidly creates a wedge-shaped cut in the wafer surface to reveal internal interfaces and profiles. This technique exposes buried features, enabling process and metrology engineers to directly identify incomplete etching, bowing, twisting, and CD variations between the top and bottom of the stack. Measurements can be quickly performed and analyzed to better understand and adjust process performance.

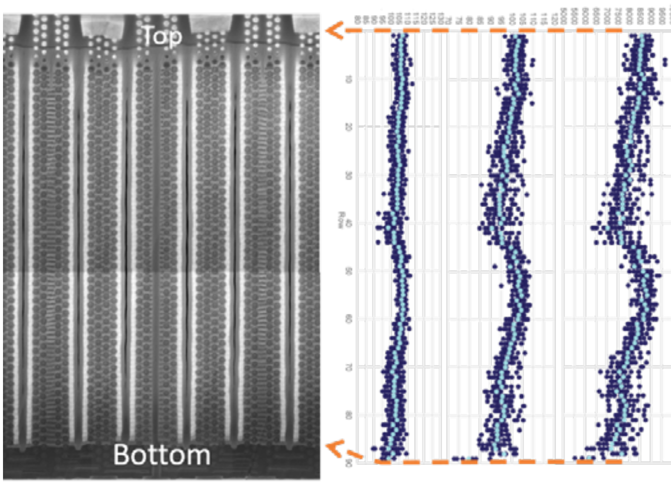

Figure 5. Full-stack 3D SEM metrology using the Helios 5 PXL PFIB Wafer DualBeam.

The Helios 5 PXL PFIB Wafer DualBeam can also deprocess 3D NAND structures. This technique involves the layer-by-layer removal of material combined with SEM imaging and metrology to measure CDs from the top to the bottom of the memory stack. This technique yields thousands of CDs per location, allowing for the complete statistical analysis of critical process performance metrics like bow CD, twist, tilt, and taper for that site.

Designed to meet the in-line metrology and process control requirements of the fab, the Helios 5 PXL PFIB Wafer DualBeam significantly reduces time to data and enables the wafer to be returned to the line without being scrapped. The instrument is compatible with semiconductor factory automation, facilitating operator-free, recipe-driven operations to support the high-throughput metrology requirements of the fab.

Conclusion: Metrology must continue to innovate

Data demands across a range of applications are creating increased performance and capacity requirements for memory technology. To provide higher bit-densities, 3D NAND manufacturers are racing to provide devices with more layers and taller structures. With each generation, the fabrication of 3D NAND becomes more complex.

A critical component for the 3D NAND manufacturing process is metrology. Unfortunately, legacy 2D planar NAND metrology solutions have limitations in measuring CDs in 3D NAND due to the structure of the memory layers, especially in the middle regions and the bottoms of the stacks.

This white paper discusses the need for new metrology techniques to measure CDs of HAR structures, inspect buried features, and provide accurate data for process improvements. Specifically designed to meet the in-line metrology and process control requirements of the fab, the Helios 5 PXL PFIB Wafer DualBeam is compatible with semiconductor factory automation, facilitating operator-free recipe-driven operation to accelerate acquisition of critical data to support 3D NAND design and high-volume manufacturing.

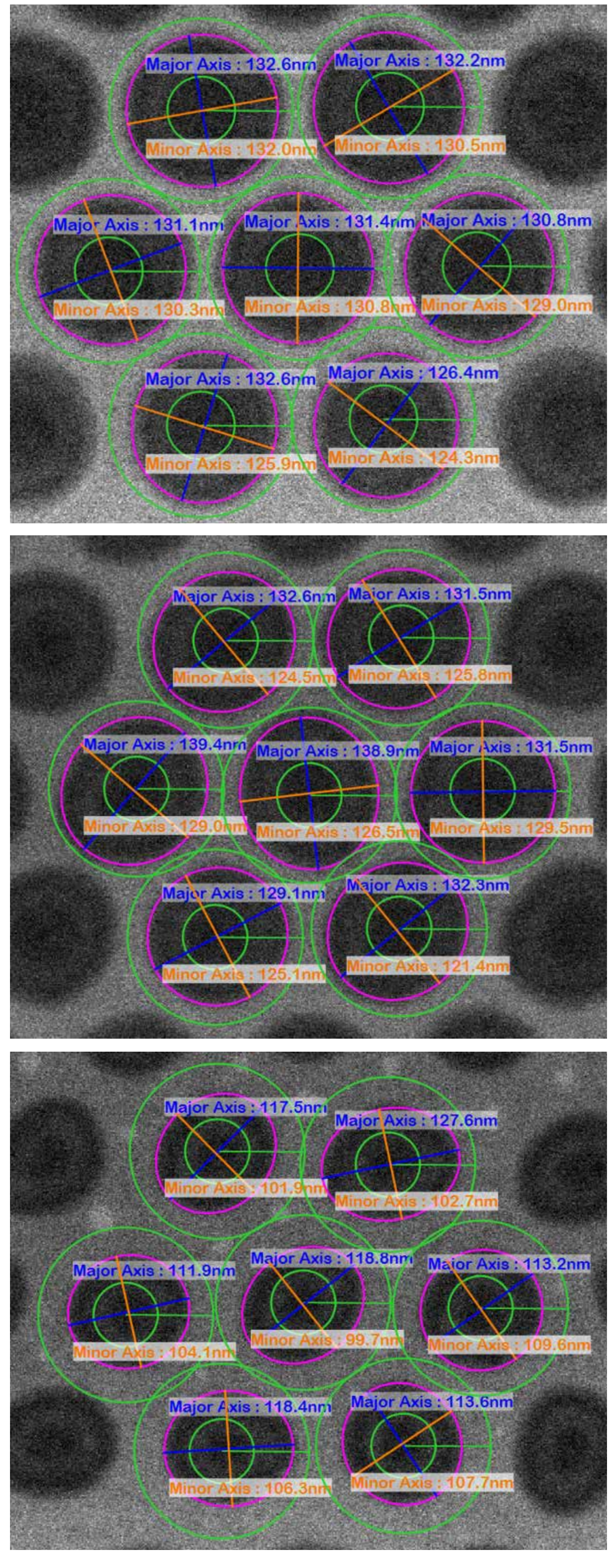

Figure 6. Layer-by-layer deposition of 3D NAND channel holes. Top, middle, and bottom layers.

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Your next step

To find out more about how fab process owners can quickly access buried CDs in 3D NAND (without transferring to a metrology lab) using the Helios 5 PXL PFIB Wafer DualBeam, visit www.thermofisher.com/Helios-5-PXL or contact your Account Manager.

About us

Thermo Fisher Scientific provides workflows for semiconductor failure analysis, characterization, metrology, and research labs to meet the needs of analog, MEMS, logic, memory, foundry, packaging, and display applications. Our solutions include automated, high-productivity TEM/TEM sample prep that provides zero-damage, low-z imaging and characterization; innovative chemical, electrical, and physical failure analysis; and compliance testing systems to localize subtle electrical issues that affect yield, performance, and reliability.

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