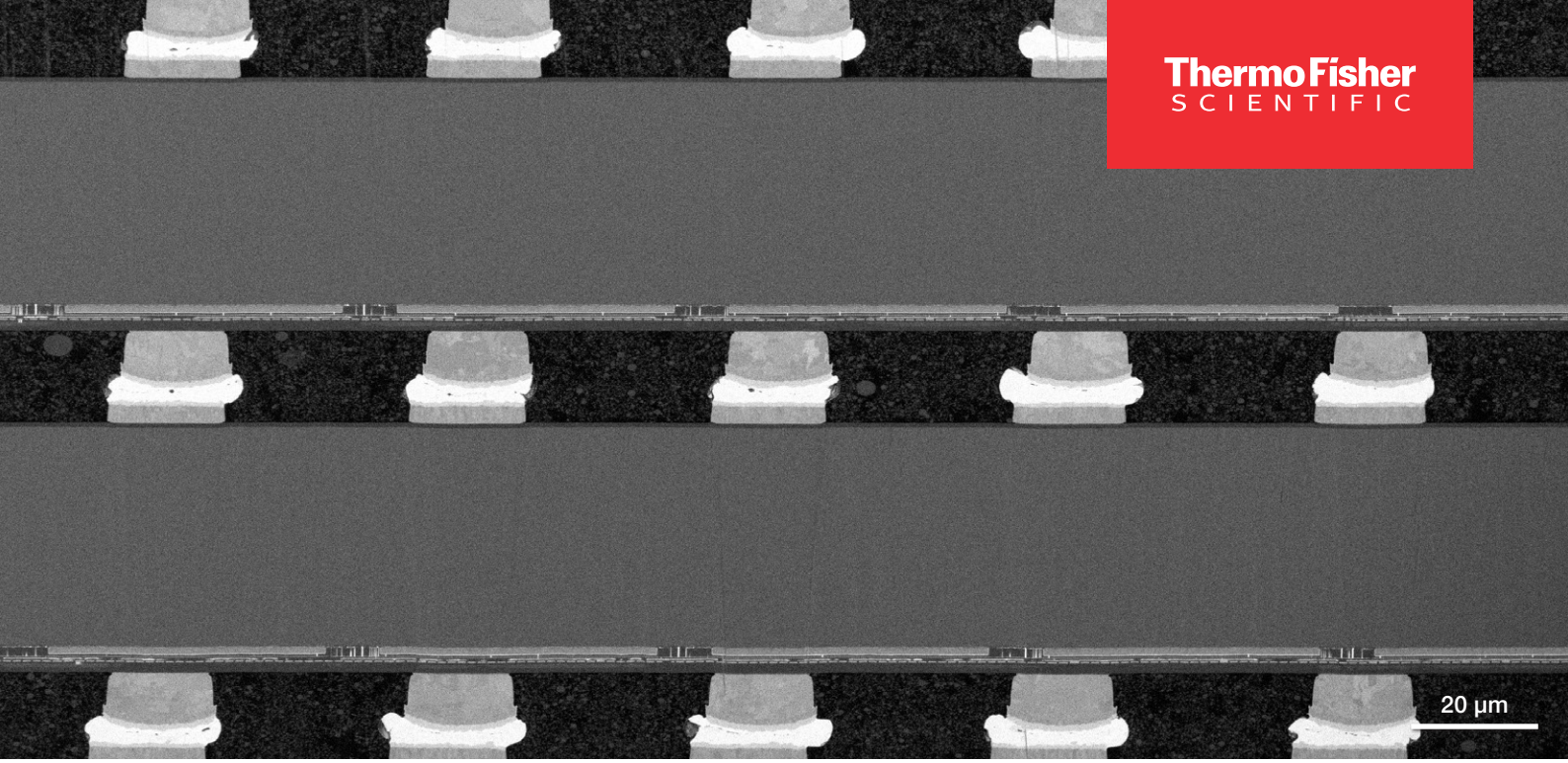


Innovative failure analysis solutions for advanced packaging

Tools, techniques, and emerging solutions

Authors

Sam Lin,
Thermo Fisher Scientific TW

Trevan Landin,
Thermo Fisher Scientific USA

Keywords

Advanced packaging, 2.5D, 3D, Wafer-level packaging, heterogeneous integration, failure analysis, defect, interconnect degradation, delamination, electromigration, non-destructive, destructive, X-ray computed tomography (XCT), scanning acoustic microscopy (SAM), lock-in thermography (LIT), focused ion beam (FIB) analysis, transmission electron microscopy (TEM)

Introduction

As semiconductor technology advances, the demand for high-performance, power-efficient, and miniaturized devices is rapidly growing. Advanced packaging technologies, such as 2.5D, 3D integration, wafer-level packaging (WLP), and heterogeneous integration, play a crucial role in enabling these innovations. However, as packaging structures become more complex, new reliability challenges and failure mechanisms emerge, necessitating sophisticated failure analysis (FA) methodologies. FA is critical for identifying defects, improving yield, ensuring product reliability, and reducing time-to-market for semiconductor manufacturers.

This white paper explores the evolving landscape of FA in advanced packaging, detailing the most common failure mechanisms, including interconnect degradation, delamination, electromigration, and thermal-induced stress. It examines cutting-edge FA techniques—both non-destructive and destructive—such as X-ray computed tomography (XCT), scanning acoustic microscopy (SAM), lock-in thermography (LIT), focused ion beam (FIB) analysis, and transmission electron microscopy (TEM).

Despite advancements in FA tools, the miniaturization of semiconductor devices presents new challenges, such as limited accessibility to buried interconnects, complex material interactions, and increased failure mode variability. The industry is responding by developing real-time monitoring techniques, high-resolution imaging solutions, and advanced simulation models to enhance reliability assessments.

Through case studies and industry insights, this white paper highlights the best practices for FA in advanced packaging, and it outlines future directions for the field. As semiconductor packaging continues to evolve, a proactive approach to FA will be essential in ensuring product quality, optimizing manufacturing processes, and driving innovation in next-generation electronic devices.

Introduction to advanced packaging

Evolution of semiconductor packaging

The semiconductor industry has undergone a significant transformation in packaging technologies over the decades, driven by the increasing demand for higher performance, power efficiency, miniaturization, and heterogeneous integration. Traditionally, packaging primarily served as a protective enclosure and provided electrical connections between the semiconductor die and the system board. However, as device scaling under Moore's Law reached physical and economic limits, advanced packaging techniques emerged as a key enabler of continued performance improvements, higher integration density, better power efficiency, and enhanced functionality beyond the capabilities of traditional monolithic scaling.

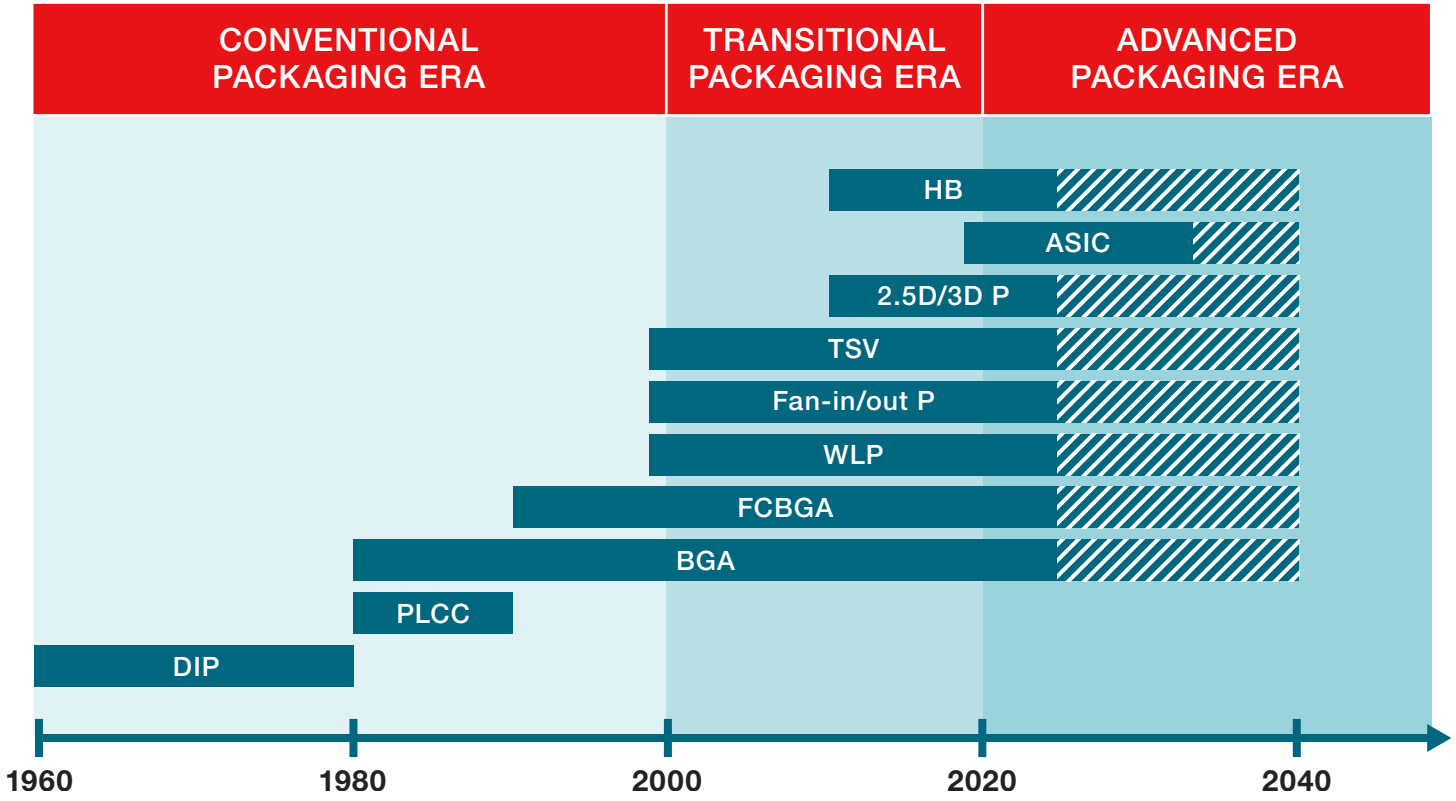
We can broadly categorize the timeline into key eras of packaging history **(Figure 1):** conventional, transition, and advanced. These eras are not defined by a single event but rather by a gradual industry transition driven by increasing performance demands, miniaturization, and heterogeneous integration needs.

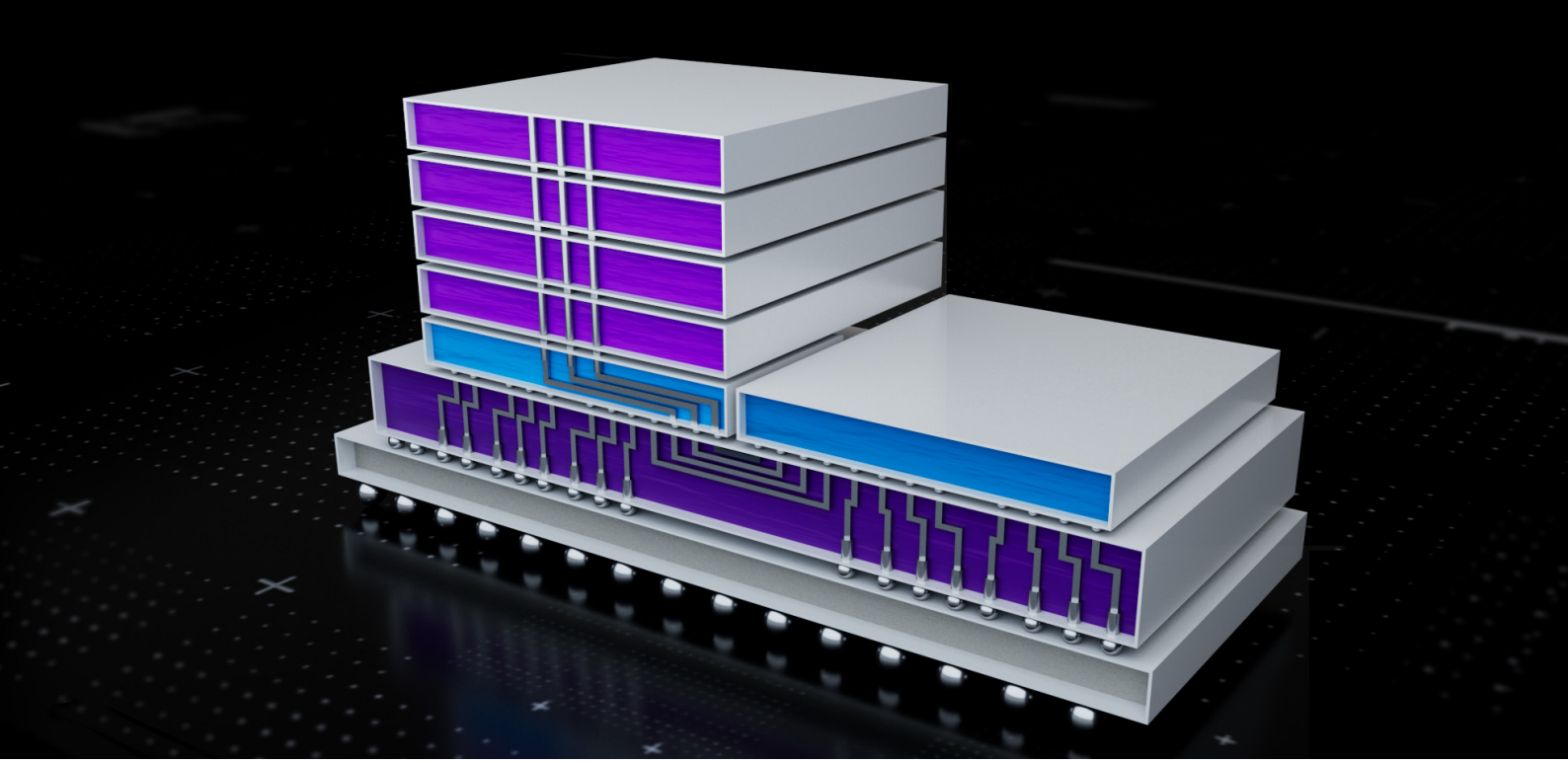
During the conventional packaging era (before the early 2000s), semiconductor packaging primarily served as a mechanical enclosure and electrical interface for the chip. Key driving factors included cost-efficiency, manufacturability, reliability, and compatibility with standard PCB technologies. Representing techniques from this era include wire bonding, lead frame-based packaging, and single-die integration[1 2 3 4].

However, as computing, telecom, and mobile applications evolved, the industry faced interconnect, thermal, and miniaturization challenges that traditional packaging could no longer address. This led to the rise of wafer-level packaging, Fan-in and Fan-out packaging, and through-silicon vias (TSVs) from the mid-2000s to the early 2010s, and we can name this as the transition packaging era[5 6 7].

The advanced packaging era (mid 2010s to present) builds upon the transition packaging era's innovation, including 2.5D and 3D packaging[8], chiplet-based architectures[9], and hybrid bonding[10] techniques to address the higher functional challenges of AI, IoT, and 5G communications. The industry is now focused on heterogeneous integration, fan-out wafer-level packaging (FOWLP), and silicon interposers for high-performance applications. The rise of 2.5D and 3D packaging, along with high-bandwidth memory (HBM) and AI accelerators, has solidified advanced packaging as the key enabler of modern semiconductor technology.

Figure 1. Packaging era and the representing techniques. Dual in-line package (DIP), plastic leaded chip carrier (PLCC), ball grid array (BGA), flip-chip ball grid array (FC-BGA), wafer-level packaging (WLP), fan-in and fan-out packaging, through-silicon vias (TSVs), application-specific integrated circuit (ASIC), and hybrid bonding (HB) are displayed in this figure[5 6 7 8 9 10 11 12 13 14].





Advanced Semiconductor Packaging: Bringing Stacked Chips Together

Defining advanced packaging

Unlike conventional packaging, which primarily serves as a mechanical protective enclosure and electrical interconnect interface, advanced packaging actively contributes to system performance by facilitating heterogeneous integration, high-bandwidth communication, and improved thermal management[11]. By leveraging technologies such as 2.5D interposers, 3D stacking, wafer-level packaging (WLP), fan-out packaging, and chiplet-based architectures, manufacturers can achieve higher performance-per-watt ratios, reduced signal latency, and smaller form factors while optimizing production costs.

A key advantage of advanced packaging is the ability to integrate multiple dies, often fabricated at different technology nodes, into a single package. This heterogeneous integration approach allows logic, memory, analog, and RF components to coexist, offering a significant advantage over traditional monolithic system-on-chip (SoC) designs. For instance, 2.5D packaging, which employs a high-performance silicon interposer, enables efficient inter-die communication with minimal signal delay, making it ideal for high-performance computing (HPC), AI, and networking applications[12]. Similarly, 3D stacking with TSVs facilitates vertical integration of multiple dies, significantly increasing bandwidth and reducing power consumption in memory-intensive applications, such as HBM (high-bandwidth memory) in GPUs and AI accelerators[3].

Key technologies under the advanced packaging umbrella:

- **Fan-out wafer-level packaging (FOWLP)**—Used in mobile and AI processors.
- **2.5D packaging**—Uses a silicon interposer for high-bandwidth memory (HBM) integration.
- **3D integration**—Uses through-silicon vias (TSVs) to stack logic and memory dies.
- **Chiplet architectures**—Modular approach enabling higher yield and cost efficiency.

However, these advancements introduce new manufacturing, reliability, and FA challenges. As interconnect pitches shrink and packaging architectures become more complex, reliability concerns such as delamination, electromigration, interconnect failures, and thermal stress become more prevalent. For example, TSV-induced stress can lead to silicon cracking, while fine-pitch microbumps in 2.5D/3D packaging are more susceptible to electromigration under high-current densities[4,7]. Material mismatches: Coefficient of thermal expansion (CTE) differences cause delamination and cracking[10]. Failure detection: Traditional FA methods struggle with nanoscale defect identification, leading to increased demand for AI-driven failure analysis tools[14]. Addressing these issues requires not only robust design methodologies and material innovations but also cutting-edge FA capable of detecting and characterizing defects at the nanometer scale. FA methodologies must evolve, incorporating high-resolution imaging (X-ray CT, IR, SEM, TEM), machine learning-driven defect detection, and *in situ* reliability monitoring. As 5G, AI, and quantum computing drive demand for higher performance and reliability, FA and reliability engineering will become even more critical to sustaining progress in advanced packaging technologies.

Failure mechanisms in advanced packaging

Advanced packaging and its challenges

As advanced packaging technologies evolve to enhance performance, power efficiency, and integration, they introduce new failure mechanisms that impact reliability, manufacturability, and long-term device performance. **Figure 2** illustrates an advanced packaging device and highlights key failure mechanisms within its structure.

The left portion of **Figure 2** presents an advanced packaging structure used in high-performance semiconductor devices. This structure consists of multiple layers, including HBM, a vertically stacked memory architecture that enhances data bandwidth and power efficiency. It is interconnected to the logic dies using Cu TSV and microbumps. These logic dies (active processing units responsible for computation and data processing) are mounted onto an interposer, which acts as a bridge between the stacked dies and the printed circuit board (PCB). This architecture enables high-density interconnection, low latency, and enhanced power efficiency. However, due to its complexity, various manufacturing defects and reliability challenges can arise during fabrication and assembly. The interposer is a silicon-based intermediary layer that provides routing between logic dies and the PCB. The interposer helps reduce signal latency and enables efficient integration of multiple dies. C4 bumps and BGA form the connection between the interposer and the PCB . BGA enables a robust mechanical and electrical interface between the package and the system board. Despite its advantages, several critical challenges arise in this multi-layered packaging architecture due to material integration, electrical interconnect reliability, structural integrity and the buried undesirous defects.

The right part of **Figure 2** displays several defects and challenges can arise within different parts of this packaging structure. These challenges highlight the importance of advanced inspection and metrology techniques to maintain high yield and reliability in semiconductor packaging.

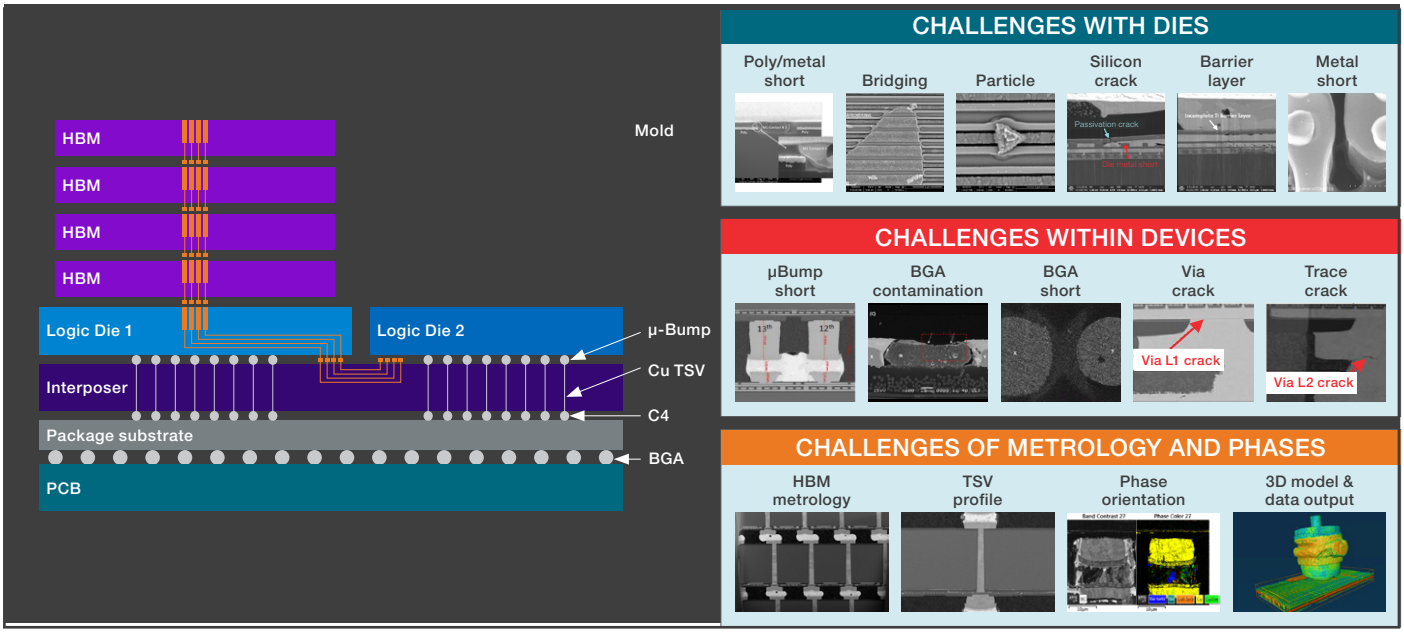
Challenges within dies

Defects such as poly/metal short circuits[15], bridging[16], particle contamination[17], silicon cracks[18], barrier layer defects[19],and metal shorts[20] affect the yield and functionality of semiconductor dies. These defects result from manufacturing process variations, material imperfections, and stress-induced failures. These defects must be detected early in the fabrication process using optical and electron microscopy, electrical testing, and failure analysis techniques to maintain high device yield and reliability.

Challenges within devices

Once the dies are packaged into a complete system, interconnect-related failures can arise due to mechanical stress, contamination, or bonding issues, potentially leading to connectivity failures that reduce the reliability and durability of the final packaged device. Common defects include micro-bump shorts[21], BGA contamination[22], BGA shorts[23], via cracks[24], and trace cracks (microcracks)[25]. These defects necessitate reliability testing methods such as X-ray inspection, cross-sectional analysis, and thermal cycling tests to ensure robust interconnect performance and long-term device durability.

Figure 2. Illustration of the advanced packaging structure and the associated challenges.



Challenges in metrology and material phase characterization

Given the complexity of advanced packaging, metrology and material phase analysis are essential for quality control and process optimization. These techniques help detect structural defects, optimize material composition, and ensure proper alignment of different layers within the package. Key challenges include HBM metrology[26], TSV profile analysis[27], phase orientation study[28] and 3D modeling and data output[29]. By leveraging these metrology and phase characterization techniques, manufacturers can enhance device performance, improve yield, and ensure long-term reliability in advanced semiconductor packaging.

Failure mode in advanced packaging

Electromigration (EM) in microbumps and redistribution layers (RDLs)

Electromigration occurs when high current densities cause metal atoms to migrate, leading to void formation, open circuits, or short circuits in micropumps, TSVs, and RDLs[30]. This failure can be found in 2.5D interposers and 3D stacked dies using microbumps, FOWLP using thin RDLs, and HB interconnects. Finally, it impacts timing failures due to resistance increase, interconnect degradation and chip failure, and thermal acceleration worsening the issue.

Thermal and mechanical stress-induced failures

Coefficient of thermal expansion (CTE) mismatch

In order to meet certain designs, different materials, like metal, semiconductor, ceramic, polymer, are often employed in interposers, substrates, underfill, and solder joints. These materials can expand and contract at different rates under thermal cycling, leading to delamination and cracking[31]. This CTE mismatch could happen at 2.5D and 3D ICs with organic or silicon interposers, FOWLP, and heterogeneous integrations. Subsequently, the die cracking and delimitation, mechanical stress leading to fatigue failures, and degraded thermal performance and reliability reduction were inevitable.

Warpage and die cracking

Warpage and die cracking[32] have become critical challenges as semiconductor packages continue to shrink in thickness and expand in size. Internal stress, induced during processes such as reflow soldering, underfill curing, and thermal cycling, can cause significant warpage, leading to die cracking, interconnect breakage, and assembly defects. This issue is particularly prevalent in large FOWLP and 3D IC packages, as well as in chiplet-based architectures that incorporate heterogeneous materials. The resulting deformation can cause bonding failures, misalignment, and increased mechanical stress on interconnects, ultimately leading to higher manufacturing defects and reduced yield. Addressing these challenges requires advanced material engineering, optimized thermal management, and improved process controls to ensure long-term package reliability.

Interconnect and solder joint failures

Microbump and HB failures

Microbump interconnects in advanced packaging technologies are highly susceptible to electromigration, void formation, and crack propagation, which can compromise device reliability over time. Similarly, HB defects often arise due to misalignment or insufficient bonding strength, leading to structural weaknesses in interconnects[33]. These issues are particularly critical in 3D IC stacking, such as high-bandwidth memory (HBM) and logic-on-memory architectures, as well as in HB-based chiplets, in which precise alignment and robust connections are essential for high-performance computing. The resulting failures can lead to open circuits, degraded performance, and increased power consumption due to higher contact resistance, ultimately affecting the efficiency and lifespan of the packaged device. To mitigate these challenges, improvements in bonding technology, material selection, and process optimization are essential for ensuring long-term reliability.

Solder joint fatigue and whisker growth

Solder joints in advanced packaging technologies are highly susceptible to thermal cycling and mechanical stress, which can lead to crack formation and eventual joint failure over time. Additionally, the use of lead-free solder introduces the risk of tin whisker growth, which can cause unintended electrical shorts and reliability concerns[34]. These challenges are particularly significant in FC-BGA, FOWLP, and other flip-chip interconnects, where mechanical and thermal stresses are more pronounced. The consequences of solder joint failures can be severe, resulting in sudden malfunctions in power devices and high-performance computing (HPC) chips, as well as field failures in critical applications such as automotive and aerospace electronics. To enhance reliability, advanced solder materials, optimized reflow processes, and conformal coatings are being explored to mitigate these risks.

TSV reliability issues

TSVs introduce localized stress in silicon, which can result in microcracks, mobility shifts in transistors, and overall performance degradation[35]. This issue is particularly critical in 3D-stacked memory and logic chips, as well as image sensors that rely on TSV-based interconnects for high-density integration. The mechanical stress exerted by TSVs can alter transistor characteristics, leading to variability in electrical performance, reduced reliability, and lower device yield.

These shifts in transistor behavior can significantly impact circuit operation, particularly in high-performance applications where precision and stability are essential. To mitigate TSV-induced stress, advanced design methodologies, stress-relief techniques, and optimized material selections are being explored to improve the robustness of 3D-integrated systems.

Delamination and underfill voiding

Poor adhesion and void formation in underfill materials pose significant reliability challenges, leading to delamination, interconnect failure, and degraded thermal performance in advanced semiconductor packaging[36]. These issues are particularly prevalent in 3D ICs, advanced flip-chip packages, and high-power processors for AI and HPC, where effective thermal management and mechanical stability are critical. Insufficient underfill integrity can result in reduced thermal dissipation, causing overheating and accelerated material degradation, ultimately compromising device longevity. Additionally, void-induced stress can lead to interconnect degradation over time, increasing the risk of electrical failures. To address these concerns, improvements in underfill formulation, enhanced adhesion techniques, and optimized curing processes are essential for ensuring the reliability of next-generation electronic systems.

Signal integrity and power integrity issues

As signal frequencies exceed 10 GHz in 5G, AI accelerators, and HPC applications, signal integrity challenges become increasingly critical. Issues such as crosstalk, power noise, and ground bounce emerge due to the use of high-density interconnects and ultra-thin redistribution layers (RDLs) in advanced packaging[37]. These challenges are particularly significant in 2.5D HBM integration and fan-out packaging for RF applications, where precise signal transmission is essential for optimal performance. Poor signal integrity can lead to increased bit error rates (BER) in high-speed interfaces, ultimately degrading system efficiency and reliability. Additionally, interference-related losses can severely impact the performance of AI and 5G systems, necessitating advanced design techniques, improved electromagnetic shielding, and optimized power delivery networks to mitigate these effects.

Failure analysis techniques for advanced packaging

Non-destructive techniques

X-ray computed tomography

XCT is a non-destructive imaging technique used in semiconductor packaging to inspect internal structures, detect defects, and analyze material properties. It enables 3D visualization of complex packaging architectures, including TSVs, microbumps, RDLs, and underfill voids, without requiring physical cross-sectioning. Key applications include solder joint inspection, HB failure detection, and void analysis in FOWLP, 2.5D interposers, and 3D ICs[38]. Engineers use micro-CT (~1 µm resolution), nano-CT (~50 nm resolution), and dual-energy XCT to analyze defects, differentiate materials, and optimize manufacturing[39]. While versatile, XCT struggles with high-density logic chips at ≤5 nm nodes[40].

Resolution varies: Micro-CT for package inspection, nano-CT for interconnect defects, and dual-energy XCT for material differentiation[41]. However, high-density semiconductor devices pose several challenges. Advanced logic chips (e.g., 5 nm and below) contain ultra-fine interconnects and dense metal layers that strongly absorb X-rays, causing image artifacts and limiting penetration[42]. Additionally, beam hardening effects, diffraction-induced distortions, and poor contrast in low-Z materials (e.g., polymers, oxides) make it difficult to accurately analyze deep-layer structures[43]. The trade-off between scan time and resolution is another challenge. While high-resolution nano-CT scans provide better detail, they can take over an hour per sample, making them impractical for high-volume manufacturing (HVM) defect detection[44]. Therefore, while XCT is highly effective for package-level defect inspection (TSVs, solder joints, and voids), it is not suitable for sub-10 nm interconnect analysis in high-density logic chips, where techniques like TEM, SEM, and FIB remain essential for nanoscale defect characterization[45].

Scanning acoustic microscopy

SAM is a non-destructive ultrasonic imaging technique used in semiconductor packaging to detect internal defects such as delamination, voids, cracks, and adhesion failures within multi-layered structures. SAM operates by transmitting high-frequency ultrasound waves (typically in the MHz to GHz range) into the sample. These waves interact with different material layers and interfaces, where they undergo reflection, refraction, and scattering based on the acoustic impedance differences between materials. A piezoelectric transducer detects the returning echoes, which are processed to generate high-resolution images of the internal structure of the package.

Four SAM scanning modes are employed in advanced packaging. C-mode (C-SAM) provides a top-down 2D view, commonly used for detecting voids and delamination in molding compounds and underfill. B-mode (B-SAM) offers cross-sectional imaging to analyze bond interfaces and cracks within solder joints and die attach layers. A-mode (A-SAM) is used for depth profiling to measure defect depth and material thickness variations. Through-scan mode transmits waves completely through the sample, which is useful for inspecting interconnects and buried layers in FOWLP and 3D ICs. SAM is particularly effective for detecting defects in encapsulants, solder bumps, adhesives, and underfill layers, making it a critical tool for reliability assessment in 2.5D interposers, 3D-stacked ICs, and heterogeneous integration.

The resolution of SAM depends on the ultrasound frequency used. Low-frequency SAM (10–50 MHz) provides deeper penetration but lower resolution (~50 µm) and is suitable for detecting bulk delamination and large cracks in flip-chip BGAs, power modules, and substrates. Medium-frequency SAM (100–300 MHz) provides resolution in the 10–30 µm range and is used for underfill voids, die attach defects, and encapsulant failures in fan-out packages and 2.5D interposers. High-frequency SAM (500 MHz–2 GHz, ultra-high-resolution SAM (UHR-SAM)) achieves sub-micron resolution (~0.5–1 µm), allowing inspection of thin RDLs, microbumps, and HB defects in 3D ICs; however, at higher frequencies, penetration depth decreases, making it difficult to inspect deeper layers in thick substrates and stacked dies.

Lock-in thermography

LIT is a non-destructive thermal imaging technique used to detect defects such as delamination, cracks, solder joint failures, and electromigration-induced hotspots in advanced semiconductor packaging. It operates by applying a modulated periodic electrical or optical stimulus to the device under test (DUT) while capturing the resulting thermal emissions using an infrared (IR) camera. The working principle of LIT is to apply a periodic heat source (such as an AC electrical current or laser pulse) to the device. The heat propagates through the material, and the thermal wave's phase and amplitude are recorded using an IR detector. By synchronizing the thermal response with the applied stimulus, defects can be precisely located even at sub-surface levels. The phase shift of the thermal wave is analyzed to distinguish between normal heat flow and areas of thermal resistance (indicating defects). LIT is particularly effective for detecting the following structures: microcracks and delamination in FOWLP and 2.5D/3D ICs, solder joint fatigue and voids in BGAs and flip-chip packaging, electromigration-induced hotspots in RDLs and TSVs, and short circuits and resistive defects in high-density logic and memory packages.

LIT's spatial resolution is determined by the thermal diffusion length, which depends on the modulation frequency of the heat source. Typical resolutions include low-frequency LIT (~0.1–10 Hz) that penetrates deeper (up to several hundred microns) but with lower lateral resolution (~50-100 µm) and is used for bulk defect detection in substrates and die attach layers; high-frequency LIT (~10–1,000 Hz) that provides higher resolution (~5–10 µm), but it is limited to near-surface defects, and is suitable for fine-pitch interconnect failures in 3D ICs and HBM; and super-resolution LIT (~1 kHz+) that can reach sub-1 µm precision, often combined with microscope optics to inspect microbumps, HB defects, and RDL issues.

Table 1 highlights the strengths and limitations of LIT, X-ray CT, and SAM for advanced semiconductor packaging non-destructive defect analysis. Among these non-destructive defect analysis methods, no single technique is perfect for all scenarios, and a multi-modal approach is often required for comprehensive failure analysis and reliability testing in 2.5D/3D ICs, FOWLP, and HBM architectures.

Table 1. Comparison of LIT, X-ray CT, and SAM for advanced packaging defect analysis.

Technique	Best for	Resolution	Depth penetration	Strengths	Limitations
LIT	Thermal hotspots, electromigration, short circuits	5-10 µm (up to sub-µm with optics)	100s of µm (dependent on modulation frequency)	Detects active heat sources, non-contact, good for failure analysis	Struggles with metal-dense areas, limited structural detail
X-ray CT	Voids, cracks, solder joint defects	Nano-CT: <100 nm, Micro-CT: ~1 µm	Several mm (depends on material and X-ray energy)	3D imaging capability, high penetration depth	Difficult to resolve low-density materials, expensive
SAM	Delamination, underfill voids, bond integrity	0.5 – 50 µm (depends on frequency)	100s of µm (depends on acoustic frequency)	Excellent for polymer and adhesive-based defects	Poor at imaging metal-dense areas, limited to surface and near-surface defects

Destructive techniques

DualBeam FIB-SEM microscopy

DualBeam™ FIB-SEM involves using a focused beam of ions (usually gallium ions) to interact with a sample surface, which is then analyzed by SEM. FIB-SEM combines two distinct techniques. With FIB, the ion beam can mill (remove material) or modify the surface of the sample. It is highly focused and can be used for deposition, precision cutting, imaging, and analysis. This makes it very useful for applications that require micro- or nanoscale precision. SEM detects secondary electrons emitted from the sample when it is bombarded by the ion beam, creating high-resolution 2D images. This provides high spatial resolution for surface morphology and elemental analysis via energy-dispersive X-ray spectroscopy (EDS) and the characterizations of crystalline orientation and phase distribution via electron backscatter diffraction (EBSD).

The working principle of DualBeam FIB-SEM is for the ion beam to mill away layers of the material in a controlled manner. As the ion beam interacts with the sample, it causes sputtering, where atoms or ions are ejected from the sample's surface. The SEM simultaneously captures high-resolution images of the exposed cross-sections, allowing for detailed imaging of internal structures. The combination of milling and imaging enables precise 3D reconstruction and analysis of the material's internal layers, which is critical for advanced packaging in semiconductor devices, such as assessing vias, interconnects, and microstructures.

While the previous non-destructive methods revealed the defects and located them, DualBeam FIB-SEM microscopy was introduced to discover the failure sites and acquire high-resolution imaging, elemental and chemical compositions, 3D analysis of complex failures, failure mode identification, detailed cross-sectional imaging, *in situ* electromechanical analysis, and more. FIB-SEM stands out as a formidable tool in the area of failure analysis for advanced packaging, offering unparalleled precision and versatility. One of its primary strengths lies in its ability to perform high-resolution imaging and site-specific sample preparation. With FIB-SEM, analysts can achieve nanometer-scale resolution, which is crucial for identifying minute defects such as voids, cracks, and delaminations within complex packaging structures. The system's capability to precisely mill and section specific areas of interest allows for detailed examination of buried layers and interfaces without damaging surrounding areas, providing a clear view of internal features and potential failure points[46,47].

Furthermore, FIB-SEM excels in three-dimensional (3D) imaging and tomography, enabling comprehensive analysis of the spatial distribution of defects. By sequentially milling and imaging layers, it is possible to reconstruct 3D models of the sample, facilitating a deeper understanding of how defects are distributed and how they interact with the overall structure. This capability is particularly beneficial for advanced packaging, where multiple layers and intricate geometries are common. Additionally, the integration of EDS with FIB-SEM allows for detailed elemental analysis, aiding in the identification of material composition and potential contamination issues. The ability to perform *in situ* experiments, such as electrical probing and mechanical testing, further enhances its utility, allowing researchers to observe the behavior of packaging under various stress conditions[48,49].

Transmission electron microscopy

TEM is an incredibly powerful tool for failure analysis, especially in the context of advanced packaging. TEM provides high-resolution imaging at the atomic scale, making it ideal for examining fine details in the microstructure of materials. This capability is crucial for identifying failure modes in advanced packaging components, such as solder joints, intermetallic compounds (IMCs), voids, and cracks. By enabling imaging at the atomic level, TEM allows for the precise observation of defects and failure sites that can lead to device failure[50].

One of the key advantages of TEM in failure analysis is its ability to investigate IMC formation in solder joints and bump interfaces, which are common failure points in advanced packaging. IMC formation is a critical failure mechanism that can lead to embrittlement, cracking, and delamination at the interface between solder and die materials or substrates[51]. With TEM, researchers can closely examine how IMCs evolve and contribute to failure at the atomic scale, providing invaluable insights into material behavior in high-stress environments.

Another critical application of TEM is the analysis of delamination and crack propagation[52] in advanced packaging. TEM is capable of visualizing stress-induced cracks at interfaces between layers and can provide information about how cracks initiate and propagate over time. This is crucial for understanding how thermal cycling, mechanical loading, and stress contribute to failure in multi-layered packages. The high-resolution capabilities of TEM allow it to detect subtle defects that could lead to catastrophic failure in packaging systems.

TEM is also equipped with EDS, enabling elemental analysis and chemical mapping at the failure sites. This combination is extremely useful for identifying material mismatches, contaminants, and oxidation that could lead to failures in advanced packaging systems. The elemental mapping capabilities of TEM allow for the detection of foreign materials, which can compromise the reliability of interconnections or bonding layers[53].

Additionally, 3D TEM tomography[54] has become a valuable tool for analyzing complex multi-layer packaging systems. By collecting a series of 2D slices and reconstructing them, 3D TEM allows for the detailed analysis of failure modes in solder bumps, vias, and other critical components. This method is particularly useful when studying defects that propagate across multiple layers in advanced packaging systems.

Lastly, *in situ* TEM enables real-time observation of failure mechanisms as they occur under various environmental conditions, such as stress, thermal cycling, and electrical biasing. This capability allows researchers to study the evolution of cracks or delamination[55] under conditions that mimic real-world device operation. By observing failures as they happen, *in situ* TEM provides unique insights into mechanical failure and material degradation in packaging structures.

In conclusion, TEM is a powerful tool for failure analysis in advanced packaging due to its ability to provide atomic-scale imaging and elemental analysis of critical failure sites. By enabling the examination of IMCs, delamination, crack propagation, and material interfaces, TEM provides invaluable information for understanding failure mechanisms at the most detailed level.

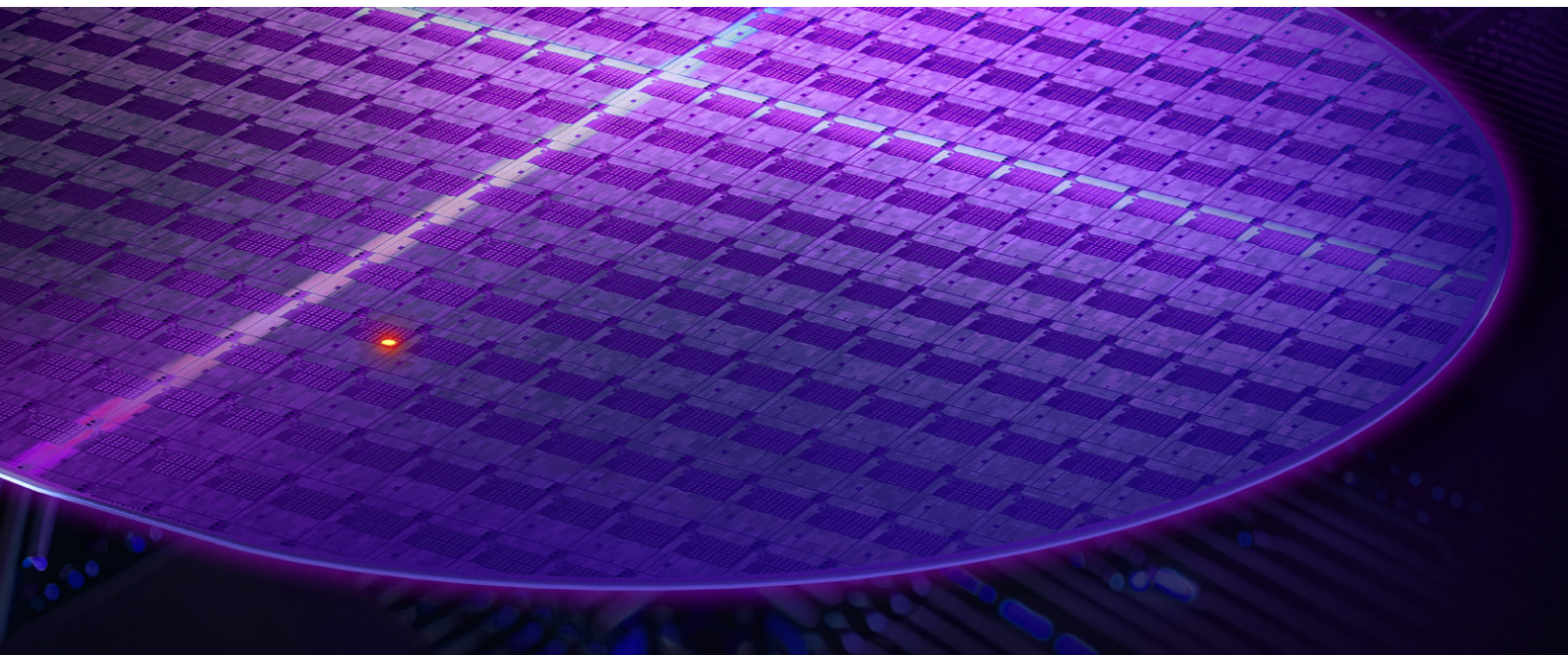
Multi-level failure analysis workflows for advanced semiconductor packaging

In the advanced packaging industry, establishing an optimal failure analysis workflow requires the integration of powerful and specialized tools at various levels of the manufacturing process, from wafer to die to device. By leveraging a suite of advanced instruments, we can ensure comprehensive and efficient analysis, ultimately leading to improved reliability and performance of packaging solutions.

At the wafer level, the Thermo Scientific ELITE™ System provides high-throughput inspection capabilities, enabling the early detection of defects and anomalies. This system is crucial for maintaining quality control and ensuring that only wafers meeting stringent standards proceed to the next stages. As we transition to the die level, the Thermo Scientific Apreo ChemiSEM™ System offers high-resolution imaging combined with rapid elemental analysis. This integration allows for precise identification of material compositions and potential contamination, facilitating targeted investigations of specific areas of interest.

For more detailed and localized analysis, the Thermo Scientific Helios™ 5 Hydra FIB-SEM comes into play. This instrument excels in site-specific cross-sectioning and 3D imaging, allowing for an in-depth examination of internal structures and interfaces within the die. The Helios 5 Hydra PFIB-SEM's capabilities are further enhanced when combined with the Thermo Scientific Talos™ (S)TEM (scanning transmission electron microscope), which provides atomic-level resolution imaging and detailed structural analysis. This combination is particularly powerful for identifying and characterizing nanoscale defects that could impact device performance.

To bring all the data together and provide a holistic view of the failure analysis, Thermo Scientific Avizo™ Software offers advanced visualization and analysis tools. Avizo Software enables the integration of data from various sources, creating comprehensive 3D models and facilitating a deeper understanding of the failure mechanisms at play. By visualizing complex structures and defects in three dimensions, engineers can better comprehend the interactions and root causes of failures.



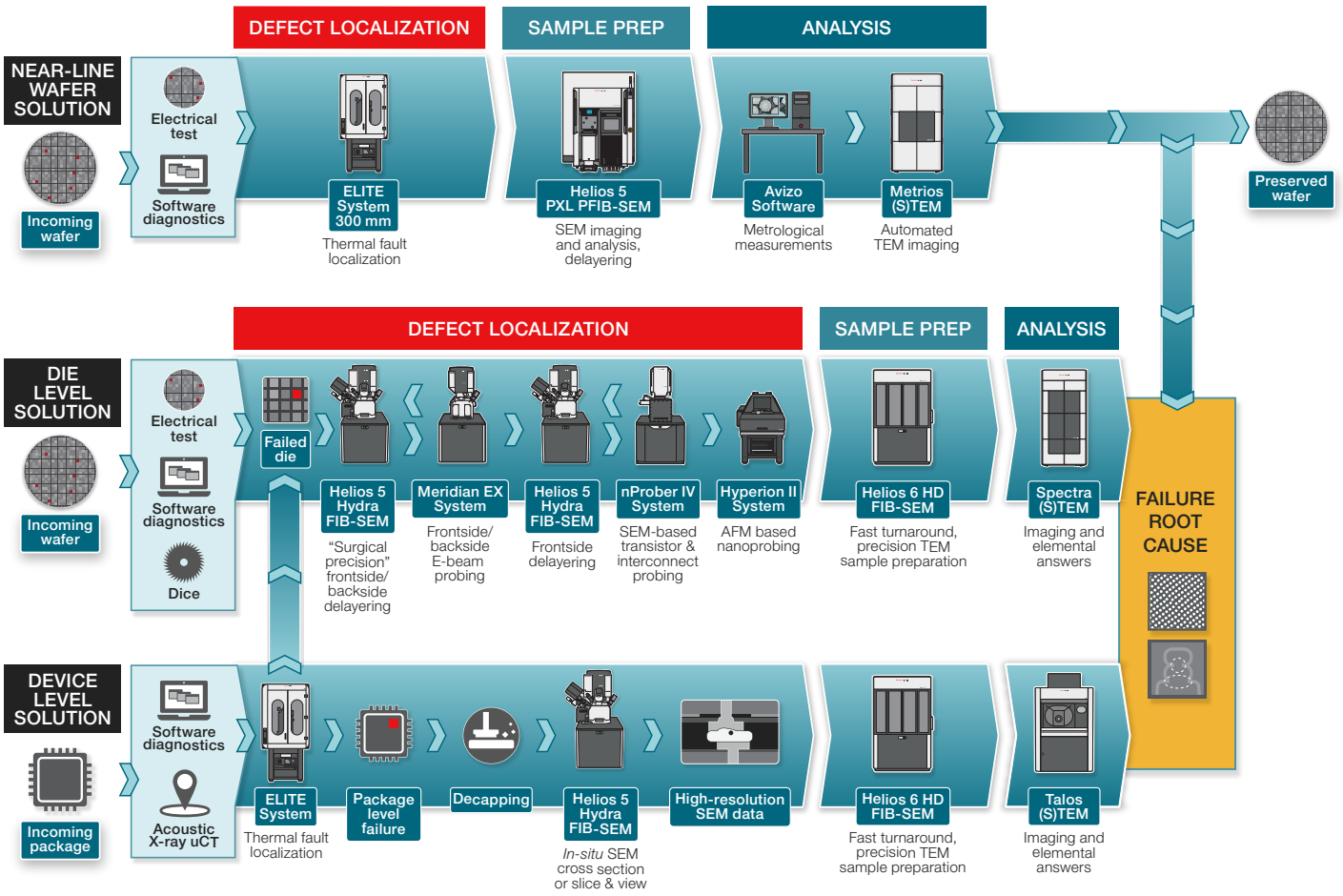


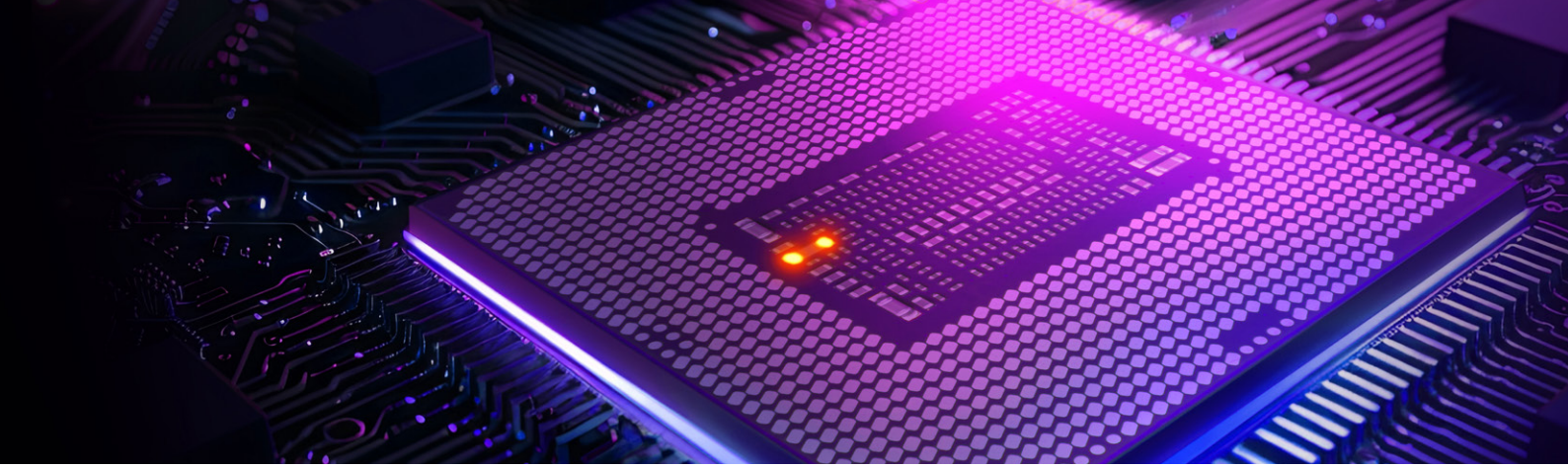
Figure 3. Multi-level failure analysis workflows for advanced semiconductor packaging.

By organizing these innovative tools into a cohesive workflow, we set an exceptional standard for failure analysis in the advanced packaging industry. This integrated approach not only enhances the accuracy and efficiency of defect identification and characterization but also accelerates the development and optimization of packaging technologies. The combined power of the ELITE System, the Apreo ChemiSEM System, the Helios 5 Hydra FIB-SEM, the Talos (S)TEM, and Avizo Software enables our workflow to be among the best, offering exceptional insights and continuous improvement in packaging reliability and performance.

Figure 3 illustrates the failure analysis process across different levels of semiconductor packaging. Each level incorporates a combination of non-destructive failure localization, sample preparation, and in-depth analysis to identify and diagnose defects efficiently.

- Near-line wafer solution focuses on 3D thermal fault localization (ELITE System 300 mm) for early defect detection while preserving the wafer. Metrology and imaging techniques such as SEM, DualBeam, and STEM are used for further structural analysis.
- Die-level solution involves electrical testing, software diagnostics, and die singulation, followed by failure localization using FIB-SEM, E-beam probing, and AFM nanoprobes. The sample is then prepped for TEM imaging to extract characteristic data and identify root causes.
- Device-level solution targets package-level defects using acoustic X-ray micro-CT and 3D thermal fault localization (ELITE System) for non-destructive failure detection. Decapping and SEM-based sample preparation enable in-depth imaging and elemental analysis with TEM.

This workflow ensures a comprehensive, multi-technique approach to semiconductor failure analysis, enhancing yield improvement and reliability in advanced packaging technologies such as 2.5D/3D ICs, FOWLP, and HBM.



Summary

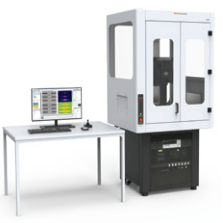
Advanced packaging failure analysis presents numerous challenges due to the increasing complexity and miniaturization of semiconductor devices. The transition to heterogeneous integration and 3D packaging has introduced significant benefits in performance and power efficiency but also presents new challenges related to manufacturing defects, interconnect reliability, and material integrity. Addressing these issues requires advanced metrology techniques, rigorous quality control, and improved material engineering. As semiconductor technology continues to evolve, AI-driven defect analysis and real-time monitoring will play a critical role in improving yield and reliability.

Building a comprehensive failure analysis workflow involves integrating various state-of-the-art tools and techniques to cover all stages of the manufacturing process, from wafer to die to device level. We have organized a comprehensive solution that addresses these complexities, offering a suite of advanced instruments and software tailored for the needs of the advanced packaging industry. At the wafer level, our ELITE System provides high-throughput inspection, helping to ensure early detection of defects. Transitioning to the die level, the Apreo ChemiSEM System combines high-resolution imaging with rapid elemental analysis, enabling precise identification of material compositions and contaminants. For localized and detailed analysis, the Helios 5 Hydra FIB-SEM excels in site-specific cross-sectioning and 3D imaging, while the Talos (S)TEM offers atomic-level resolution for detailed structural analysis.

To streamline and enhance the failure analysis process, we also offer automated Thermo Scientific software solutions such as AutoTEM™, iFast, and Avizo Software. AutoTEM Software automates the preparation of TEM samples, significantly reducing the time and effort required for high-precision analysis. iFast Software enables automated workflows for FIB-SEMs, improving efficiency and consistency in sample preparation and analysis. Avizo Software provides advanced visualization and analysis tools, integrating data from various sources to create comprehensive 3D models and facilitating a deeper understanding of failure mechanisms. These automated solutions not only enhance the accuracy and efficiency of failure analysis but also cater to versatile requests from customers, helping to ensure that their specific needs are met with precision and reliability.

By leveraging the combined power of our advanced instruments and automated software solutions, we offer a comprehensive, exceptional failure analysis workflow that addresses the intricate challenges of advanced packaging. This integrated approach helps identify and characterize defects with remarkable accuracy and efficiency, driving continuous improvement in packaging reliability and performance. Our total solution, encompassing electrical and physical failure analysis, provides the versatility and precision required to meet the evolving demands of the advanced packaging industry.

Learn more about our powerful semiconductor solutions that support advanced packaging development, manufacturing, and failure analysis.



Thermo Scientific™
ELITE System

Thermo Scientific™
Apreo ChemiSEM™
System

Thermo Scientific™
Helios™ 5 Hydra
PFIB-SEM

Thermo Scientific™
Talos™ F200S
G2 (S)TEM

Thermo Scientific™
Avizo Software

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List of Abbreviations

AI – Artificial intelligence

ASIC – Application-specific integration circuit

BER – Bit error rates

BGA – Ball grid array

CTE – Coefficient of thermal expansion

DIP – Dual in-line package

DUT – Device under test

EBSD – Electron backscatter diffraction

EDS – Energy-dispersive X-ray spectroscopy

EM – Electromigration

FA – Failure analysis

FCBGA – Flip-chip ball grid array

FIB – Focused ion beam

FOWLP – Fan-out wafer-level packaging

HB – Hybrid bonding

HBM – High-bandwidth memory

HPC – High-performance computing

HVM – High-volume manufacturing

IMC – Intermetallic compound

IR – Infrared

LIT – Lock-in thermography

PCB – Printed circuit board

PLCC – Plastic leaded chip carrier

RDL – Redistribution layer

SAM – Scanning acoustic microscopy

SoC – System-on-chip

TEM – Transmission electron microscopy

TSV – Through-silicon via

UHR – Ultra-high resolution

WLP – Wafer-level packaging

XCT – X-ray computed tomography

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