

Find hidden failures faster with the ELITE System

Accelerating electrical fault isolation in advanced semiconductor devices and packaging

Hidden cost of device complexity

Semiconductor innovation continues to drive advances in artificial intelligence, high-performance computing, automotive electronics, mobile devices, and power management. These gains are being enabled by increasingly complex device architectures that pack more functionality into smaller footprints.

Advanced packaging technologies now combine multiple dies, diverse process nodes, and heterogeneous materials into highly integrated systems. Interconnect density continues to increase while critical dimensions continue to shrink.

These advances create significant challenges for failure analysis teams:

- Signal paths span multiple buried layers
- Interconnect pitches continue to shrink
- Thermal behavior becomes increasingly difficult to interpret
- Defects may be hidden beneath micro-bumps, TSVs, redistribution layers, and stacked dies
- Traditional localization workflows become slower and less effective

As a result, finding a fault often becomes just as difficult as understanding it.

Without a fast and reliable localization strategy, root cause identification is delayed, engineering resources are consumed, and corrective actions take longer to implement.

Why fault localization matters

Every failure analysis workflow begins with the same question: **Where is the defect?**

Before engineers can perform destructive sample preparation, nanoprobng, SEM analysis, or TEM analysis, they must first identify the location of the failure.

This localization step determines the efficiency of every downstream activity.

Poor localization can lead to:

- Multiple preparation iterations
- Missed defects
- Longer cycle times
- Increased tool utilization
- Reduced engineering productivity

Effective fault localization narrows the search area quickly and accurately, enabling engineers to focus resources on understanding the root cause rather than searching for it.

As devices become more complex, the value of accurate localization continues to increase.

The goal is no longer simply detecting a failure. The goal is to rapidly identify its location with enough confidence to guide the remainder of the analysis workflow.

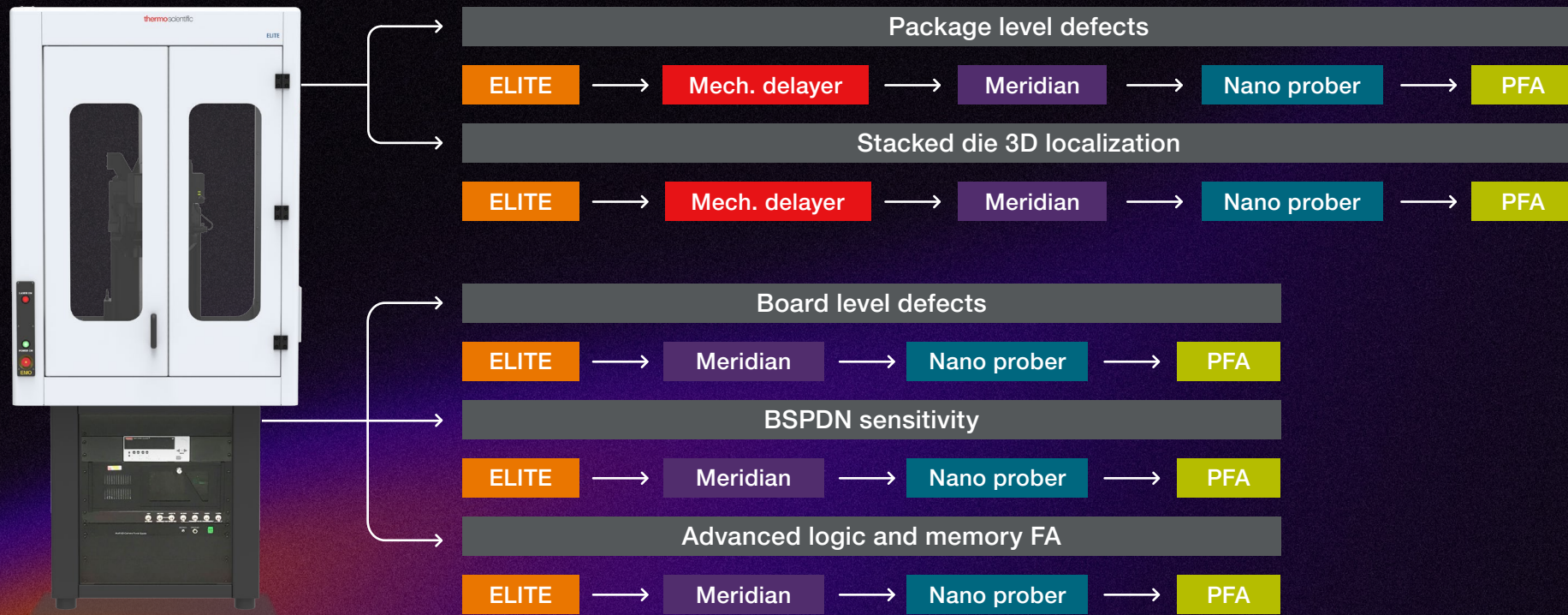
Modern electrical fault isolation workflow

Successful root cause analysis depends on a connected workflow.

Each stage builds on the accuracy and information of the previous step.

When localization is performed quickly and precisely, engineers can reduce unnecessary preparation, improve analysis efficiency, and increase confidence in final conclusions.

Especially as advanced packaging structures continue to increase in complexity, fault localization is the critical first step that determines the overall efficiency of the workflow.



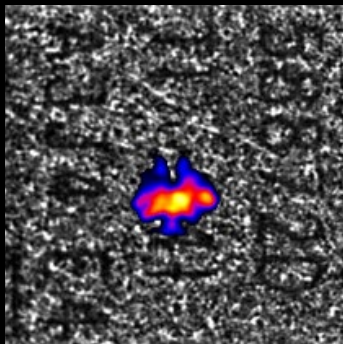
Not all defects are the same

Electrical failures occur in numerous forms.

Some defects generate heat and are easily observed through thermal detection, while others have more subtle heat signatures requiring extreme sensitivity. Others remain thermally inactive and require advanced approaches to isolate.

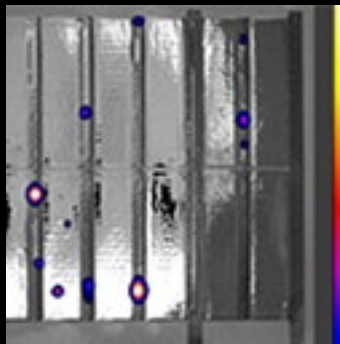
Common defect types include:

Hard shorts



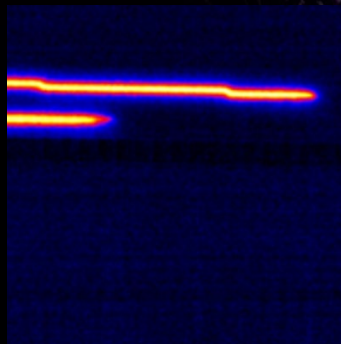
Direct electrical short circuits detected via thermal emission.

Leakage paths



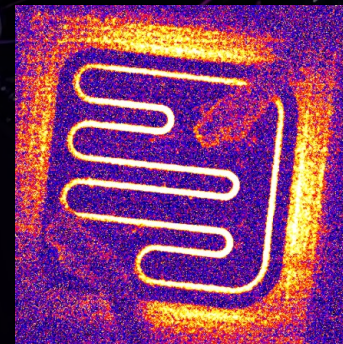
Low-resistance paths rapidly localized via strong thermal signatures.

Resistive opens



Partial interruptions in metal lines or vias identified.

High-resistance leakage



Paths localized via subtle thermal signatures stimulated by RF-LIT.

True opens



Detectable heat signatures of open traces stimulated by RF LIT.

Each failure mechanism interacts differently with electrical stimulation and thermal behavior.

Understanding which technique and parameters are best suited for a particular defect type is essential for maximizing capture rates and reducing analysis time.

Lock-in thermography: Seeing thermal defects faster

Many electrical failures generate small amounts of heat during operation. While these thermal signatures may be invisible to some inspection methods, they provide valuable clues about the location and behavior of a defect.

Lock-in thermography (LIT) is one of the most widely used electrical fault isolation techniques because it allows engineers to rapidly visualize thermally active defects with high sensitivity. Unlike other fault isolation approaches that may require multiple preparation steps, LIT allows engineers to rapidly narrow the search area while leaving the device intact for downstream analysis.

By synchronizing electrical stimulation with thermal image acquisition, LIT can isolate subtle temperature variations that would otherwise be lost in background noise.

For advanced semiconductor devices, LIT enables localization of:

- Dielectric breakdown
- Interconnect bridging
- Dendrite growth
- Solder and micro-bump failures
- Contamination-related failures

The result is faster identification of defect locations and reduced time spent searching for failures manually. In many workflows, LIT serves as the first step in narrowing a large search area into a precise region of interest.

Lock-in thermography: How it works

Lock-in thermography is a thermal fault isolation technique that detects temperature variations associated with electrical defects.

The device under test is electrically stimulated using a periodic signal while an infrared camera captures thermal emissions from the device surface. By synchronizing image acquisition with the applied stimulus, the system separates defect-related thermal signals from background thermal noise.

This process dramatically improves sensitivity, enabling detection of temperature changes that may be invisible through conventional thermal imaging methods.

Two complementary outputs are generated:

Amplitude imaging

Amplitude images reveal the strength of the thermal response. These images are used to identify hotspots associated with electrical activity and to provide a rapid indication of defect location.

Phase imaging

Phase images measure the timing of the thermal response relative to the applied electrical stimulus.

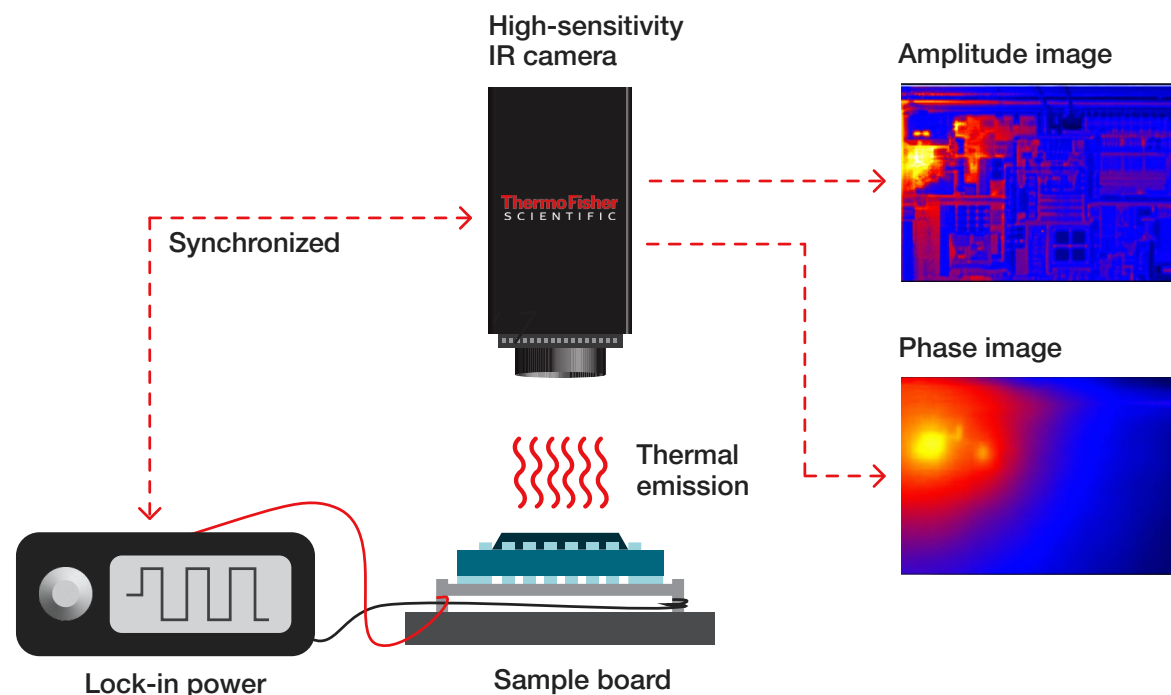
Because heat propagates through materials over time, phase information can be used to

estimate defect depth and improve localization within complex three-dimensional structures.

Together, amplitude and phase imaging provide a more complete understanding of defect location and behavior than either approach alone. Advanced algorithms further enhance this capability by calibrating thermal responses across complex package stacks, enabling accurate X, Y, and Z localization of subtle faults with high confidence.

For failure analysis teams, this means:

- Faster defect localization
- Improved capture rates
- Greater confidence in buried defect identification
- Reduced need for iterative debug cycles
- Non-destructive path toward root cause analysis



OBIRCH: Revealing subtle defects and leakage paths

Some of the most difficult failures to localize are subtle shorts and leakage paths.

These defects may not generate strong thermal signatures, yet they can significantly impact device performance, yield, and reliability.

Optical beam induced resistance change (OBIRCH) provides an effective method for isolating these challenging defects.

By scanning a focused laser across the device while monitoring electrical response, OBIRCH identifies localized resistance changes associated with defect activity.

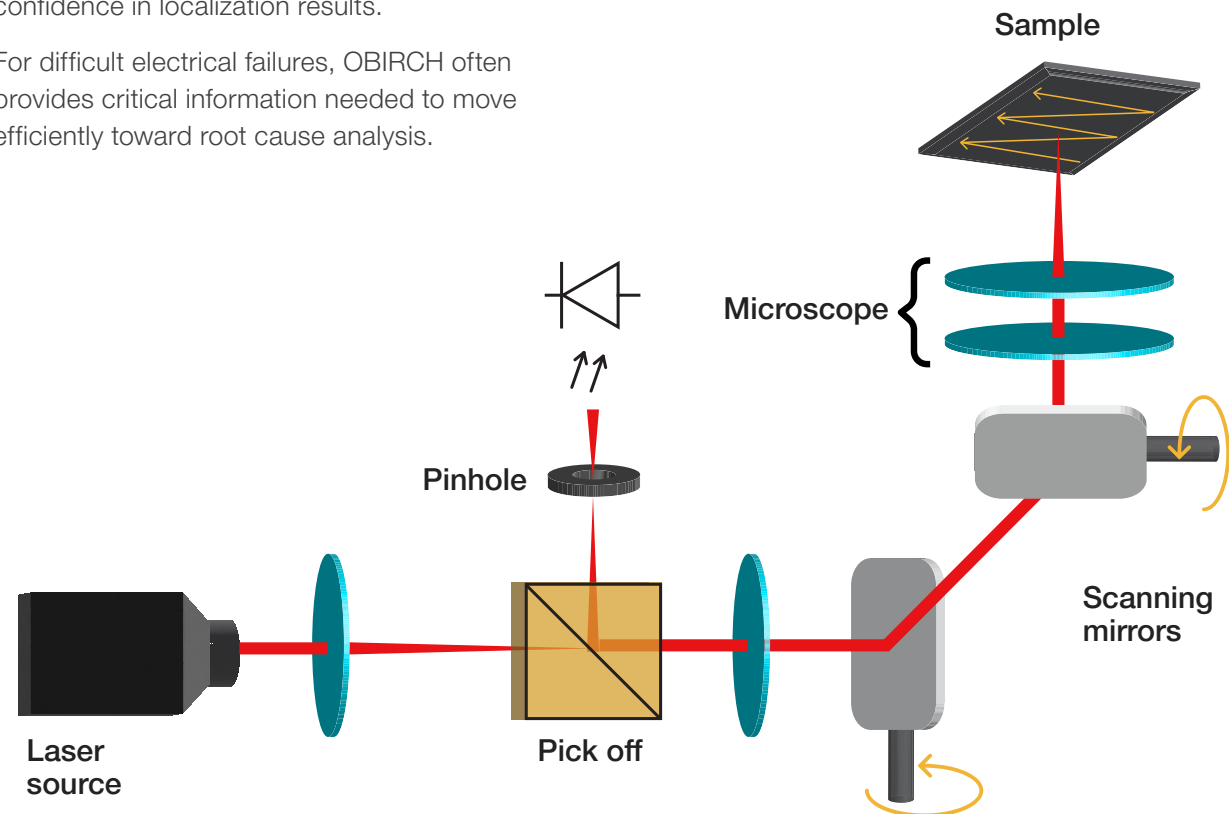
This approach is particularly effective for:

- Resistive opens
- Leakage paths

Modern OBIRCH provides significantly improved signal-to-noise performance, allowing engineers to detect defects that may have previously been hidden beneath background noise.

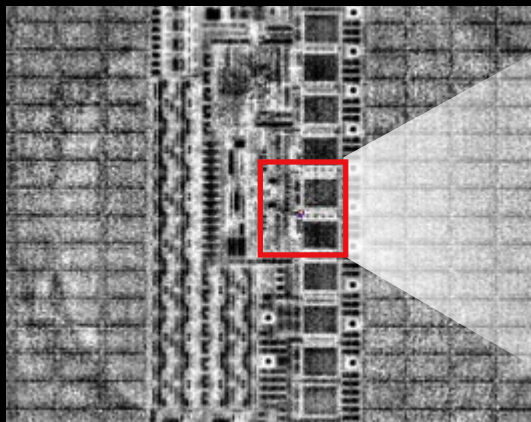
Higher sensitivity translates directly into higher capture rates, fewer missed defects, and greater confidence in localization results.

For difficult electrical failures, OBIRCH often provides critical information needed to move efficiently toward root cause analysis.

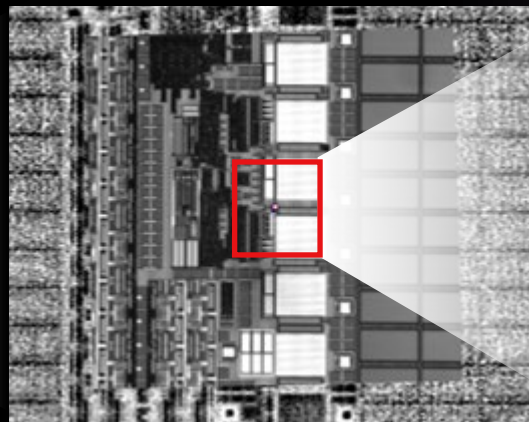


Laser scanning microscopy: Adding visual context

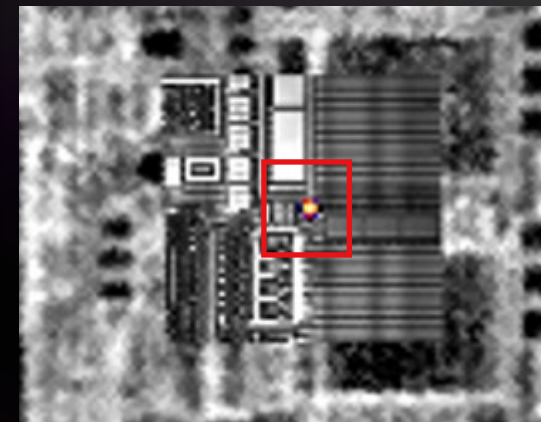
Localization is most valuable when engineers can clearly connect thermal response data to physical structures. Laser scanning microscopy (LSM) adds this critical layer of visual context.



10x hotspot overlay
on thermal 10x topography.



10x hotspot overlay on LSM 20x
overlay on thermal 10x topography.



10x hotspot overlay on LSM 100x
overlay on thermal 10x topography.

By combining LSM imaging with fault localization data, engineers can:

- Visualize defect locations within device structures
- Navigate more efficiently during analysis
- Improve re-detection accuracy
- Reduce time spent searching for localized faults
- Increase confidence before sample preparation

LSM helps transform defect data into actionable engineering insight.

RF-LIT: Localizing open faults in minutes

Not all electrical failures generate heat directly.

Open circuits, discontinuities, and broken interconnects often produce little or no thermal signature during conventional stimulation.

Radio frequency lock-in thermography (RF-LIT) addresses this challenge by applying a modulated RF signal to the device and measuring localized heating caused by discontinuities within the signal path.

RF-LIT is particularly effective for identifying:

- Open traces
- Via chain failures
- Cracks in microbumps

Because the technique highlights the location where signal transmission is interrupted, engineers can quickly isolate faults that may otherwise require extensive electrical debug.

For advanced packaging applications, RF-LIT can reduce fault localization time from hours to minutes while maintaining high confidence in the result.

As interconnect densities continue to increase, RF-LIT is becoming an increasingly important tool for identifying subtle connectivity failures hidden within complex package architectures.

One platform. Multiple fault localization techniques.

A key challenge for engineers is selecting the right technique for each failure mechanism while maintaining workflow efficiency.

The Thermo Scientific™ ELITE System brings multiple complementary fault isolation techniques together within a configurable solution designed to support a broad range of devices and applications

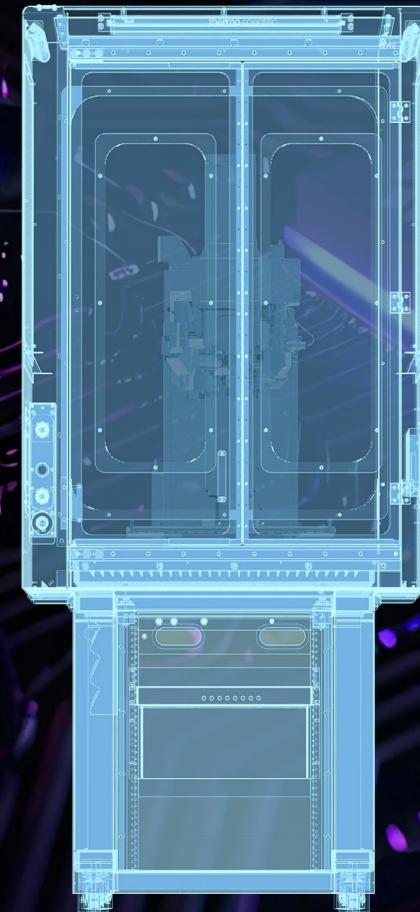
Capabilities include:

- Lock-in thermography (LIT)
- Radio-frequency LIT
- Optical beam induced resistance change (OBIRCH)

- Laser scanning microscopy (LSM)
- Thermal mapping and diagnostics
- Front and backside probing

The result is higher fault capture rates, faster localization, and greater confidence in the final result.

For organizations supporting advanced packaging, logic, memory, and power devices, a unified fault isolation platform helps reduce workflow complexity while improving engineering productivity.



Compare what matters most

Use this tool to understand compatible ELITE System configuration options:

	ELITE DX/VX System	ELITE TD System
Sample type	Packaged parts, boards	Large boards
Static stimulation	20–200 V static (DX) 1,100–10,000 V (VX)	20–200 V static
Dynamic stimulation	N/A	ATE docking Advantest
Backside probing capability Large features (>30 µm)	Flippable EDP plate Standard opening: 91 x 80 mm XL: 138 x 140 mm	Assembly required
Backside probing capability Small features (<30 µm)*	Backside probing platform 127 x 254 mm opening	N/A
Probe card support	4.5-inch cantilever	N/A
Lock-in thermography	Yes	Yes
LSM/OBIRCH	Yes	N/A
Laser marker	Yes	N/A
Thermal mapping	2 point and single point	Single point
RF-LIT for opens	Available from Q1 2027	Available from Q1 2027
Thermal camera wavelength	3.5 µm	3.5 µm

Measuring ROI beyond the tool

The value of electrical fault isolation extends far beyond the localization step itself.

Reducing localization time can generate significant operational benefits:

- Faster root cause identification
- Reduced engineering effort
- Higher utilization of downstream tools
- Increased fault capture rates
- Fewer repeated investigations
- Quicker corrective action implementation

As advanced devices become more complex, the cost of delayed fault localization continues to increase.

Organizations that can localize failures faster gain a competitive advantage through improved productivity, reduced analysis cycles, and accelerated development timelines.

Confidence in every localization decision

Electrical fault isolation is a critical capability for modern semiconductor failure analysis.

As advanced packaging, logic, memory, and power devices continue to evolve, engineers need tools that can localize failures quickly, accurately, and consistently.

The ELITE System combines advanced fault isolation techniques, high-sensitivity detection, 3D localization, and workflow flexibility within a single solution.

The result is a faster path from defect detection to root cause identification.

One platform. All electrical failures. Maximum insight.

By helping engineers localize faults with greater confidence, the ELITE System enables faster decisions, more efficient workflows, and deeper understanding of the devices that power modern technology.

Find the right configuration for your workflows today.

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